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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA – SAN JOSE DIVISION

KYOCERA COMMUNICATIONS, INC., Plaintiff, v. ESS TECHNOLOGIES INTERNATIONAL, INC. and IMPERIUM (IP) HOLDINGS, INC., Defendants.	Case No. **COMPLAINT FOR DECLARATORY JUDGMENT** [DEMAND FOR JURY TRIAL]

Plaintiff, Kyocera Communications, Inc. ("KCI"), asserts this Complaint against Defendants ESS Technologies International, Inc. ("ESSTI") and Imperium (IP) Holdings, Inc. ("IIPH") as follows:

THE PARTIES

1. KCI is a corporation incorporated under the laws of Delaware with its principal place of business at 9520 Towne Centre Drive, San Diego, California 92121.

2. Upon information and belief, ESSTI is a corporation incorporated under the laws of the Cayman Islands with its principal place of business at 48401 Fremont Blvd., Fremont, California 94538.

3. Upon information and belief, IIPH is a corporation incorporated under the laws of the Cayman Islands with its principal place of business at 515 Madison Avenue, New York, New York 10022.

JURISDICTION AND VENUE

4. This Court has subject matter jurisdiction over this action pursuant to 28 U.S.C. §§ 1331, 1338, 1367, 2201, and 2202.

5. This Court has personal jurisdiction over ESSTI. ESSTI conducts business in this District and has its principal place of business in this District.

6. This Court has personal jurisdiction over IIPH. Upon information and belief, IIPH conducts business in this District, including seeking to monetize its patent portfolio (including the patents-in-suit) in this District.

7. Venue is proper in this District pursuant to 28 U.S.C. § 1391.

INTRADISTRICT ASSIGNMENT

8. For purposes of intradistrict assignment pursuant to Local Rule 3-2(c), this Intellectual Property Action is to be assigned on a district-wide basis.

FACTUAL BACKGROUND

9. On March 30, 2011, IIPH sued KCI for patent infringement of U.S. Patent Nos. 6,271,884, 6,838,651, and 6,838,715 (collectively, the "patents-in-suit") in the United States District Court for the Eastern District of Texas.

10. U.S. Patent No. 6,271,884 (the "'884 patent") is entitled "Image Flicker Reduction With Fluorescent Lighting" and issued on August 7, 2001. Attached as Exhibit A is a copy of the '884 patent.

11. U.S. Patent No. 6,838,651 (the "'651 patent") is entitled "High Sensitivity Snap Shot CMOS Image Sensor" and issued on January 4, 2005. Attached as Exhibit B is a copy of the '651 patent.

12. U.S. Patent No. 6,838,715 (the "'715 patent") is entitled "CMOS Image Sensor Arrangement With Reduced Pixel Light Shadowing" and issued on January 4, 2005. Attached as Exhibit C is a copy of the '715 patent.

13. IIPH claims that it is the owner of the patents-in-suit.

14. Upon information and belief, IIPH is not the owner of the patents-in-suit.

15. Upon information and belief, ESSTI is the owner of the patents-in-suit.

COUNT I

(Declaratory Judgment Regarding Ownership of U.S. Patent Nos. 6,271,884, 6,838,651, and 6,838,715)

16. KCI incorporates by reference paragraphs 1 through 15 of this Complaint.

17. IIPH claims it owns the patents-in-suit.

18. Upon information and belief, IIPH does not own the patents-in-suit and does not have the right to enforce the patents-in-suit.

19. Upon information and belief, ESSTI owns the patents-in-suit.

20. An actual and justiciable controversy has thus arisen between KCI, ESSTI, and IIPH concerning the ownership of the patents-in-suit.

COUNT II

(Declaratory Judgment of Non-Infringement of U.S. Patent No. 6,271,884)

21. KCI incorporates by reference paragraphs 1 through 20 of this Complaint.

22. Upon information and belief, ESSTI is the owner of the '884 patent.

23. IIPH is asserting ESSTI's '884 patent against KCI, contending that KCI has infringed the '884 patent.

24. KCI contends that it has not infringed, and does not infringe, any valid and enforceable asserted claim of the '884 patent.

25. An actual and justiciable controversy has thus arisen between KCI, ESSTI, and IIPH concerning the alleged infringement of the '884 patent.

COUNT III

(Declaratory Judgment of Invalidity of U.S. Patent No. 6,271,884)

26. KCI incorporates by reference paragraphs 1 through 25 of this Complaint.

27. IIPH contends that the claims of ESSTI's '884 patent are valid.

28. KCI contends that the claims of the '884 patent are invalid under 35 U.S.C. §§ 101, 102, 103, and/or 112.

29. An actual and justiciable controversy has thus arisen between KCI, ESSTI, and IIPH concerning the validity of the claims of the '884 patent.

COUNT IV

(Declaratory Judgment of Non-Infringement of U.S. Patent No. 6,838,651)

30. KCI incorporates by reference paragraphs 1 through 29 of this Complaint.

31. Upon information and belief, ESSTI is the owner of the '651 patent.

32. IIPH is asserting ESSTI's '651 patent against KCI, contending that KCI has infringed the '651 patent.

33. KCI contends that it has not infringed, and does not infringe, any valid and enforceable asserted claim of the '651 patent.

34. An actual and justiciable controversy has thus arisen between KCI, ESSTI, and IIPH concerning the alleged infringement of the '651 patent.

COUNT V

(Declaratory Judgment of Invalidity of U.S. Patent No. 6,838,651)

35. KCI incorporates by reference paragraphs 1 through 34 of this Complaint.

36. IIPH contends that the claims of ESSTI's '651 patent are valid.

37. KCI contends that the claims of the '651 patent are invalid under 35 U.S.C. §§ 101, 102, 103, and/or 112.

38. An actual and justiciable controversy has thus arisen between KCI, ESSTI, and IIPH concerning the validity of the claims of the '651 patent.

COUNT VI

(Declaratory Judgment of Non-Infringement of U.S. Patent No. 6,838,715)

39. KCI incorporates by reference paragraphs 1 through 38 of this Complaint.

40. Upon information and belief, ESSTI is the owner of the '715 patent.

41. IIPH is asserting ESSTI's '715 patent against KCI, contending that KCI has infringed the '715 patent.

42. KCI contends that it has not infringed, and does not infringe, any valid and enforceable asserted claim of the '715 patent.

43. An actual and justiciable controversy has thus arisen between KCI, ESSTI, and IIPH concerning the alleged infringement of the '715 patent.

COUNT VII

(Declaratory Judgment of Invalidity of U.S. Patent No. 6,838,715)

44. KCI incorporates by reference paragraphs 1 through 43 of this Complaint.

45. IIPH contends that the claims of ESSTI's '715 patent are valid.

46. KCI contends that the claims of the '715 patent are invalid under 35 U.S.C. §§ 101, 102, 103, and/or 112.

47. An actual and justiciable controversy has thus arisen between KCI, ESSTI, and IIPH concerning the validity of the claims of the '715 patent.

DEMAND FOR JURY TRIAL

KCI demands a trial by jury of any and all issues in this action so triable.

PRAYER FOR RELIEF

WHEREFORE, KCI respectfully requests that the Court enter judgment for KCI, and award it the following relief:

A. Declare that IIPH does not own the patents-in-suit and does not have the right to enforce the patents-in-suit;

B. Declare that ESSTI is the owner of the patents-in-suit;

C. Declare that KCI has not infringed, and does not infringe, any valid and enforceable asserted claim of the '884, '651, and '715 patents;

D. Declare that the asserted claims of the '884, '651, and '715 patents are invalid;

E. Find this case an exceptional case and award KCI its attorneys' fees and costs under 35 U.S.C. § 285 and all other applicable statutes, rules, and laws; and

F. Grant KCI such other and further relief as the Court deems appropriate and just under the circumstances.

Dated: March 9, 2012

Respectfully submitted,

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EXHIBIT A

US006271884B1

(12) **United States Patent**
Chung et al.

(10) **Patent No.: US 6,271,884 B1**
(45) **Date of Patent: Aug. 7, 2001**

(54) **IMAGE FLICKER REDUCTION WITH FLUORESCENT LIGHTING**

(75) Inventors: **Randall M. Chung**, Laguna Niguel; **Magued M. Bishay**, Costa Mesa; **Joshua Ian Pine**, Seal Beach, all of CA (US)

(73) Assignee: **Conexant Systems, Inc.**, Newport Beach, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/406,964**

(22) Filed: **Sep. 28, 1999**

(51) **Int. Cl.**[7] **H04N 5/222**
(52) **U.S. Cl.** **348/370**; 348/223
(58) **Field of Search** 348/207, 208, 348/220, 222, 223, 224, 225, 226, 229, 239, 370, 371; 358/518; H04N 9/73

(56) **References Cited**

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5,239,369	*	8/1993	Suzuki	348/226
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5,384,595	*	1/1995	Sakaguchi	348/226
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Conexant Data Sheet: CNO352: Digital CMOS Imager; dated Apr. 16, 1999, Order No. 6001DSR1.

Conexant Data Sheet: CNO352p: Pixel Processor and Control Chip; dated Jun. 30, 1998, Order No. 6003DS.

USB Camera Designer's Guide: Conexant Proprietary Information; Document No. 6000DG, dated Jan. 29, 1999.

ITU–T Recommendation H.324: Terminal for low bit–rate multimedia communication, dated Feb. 1998.

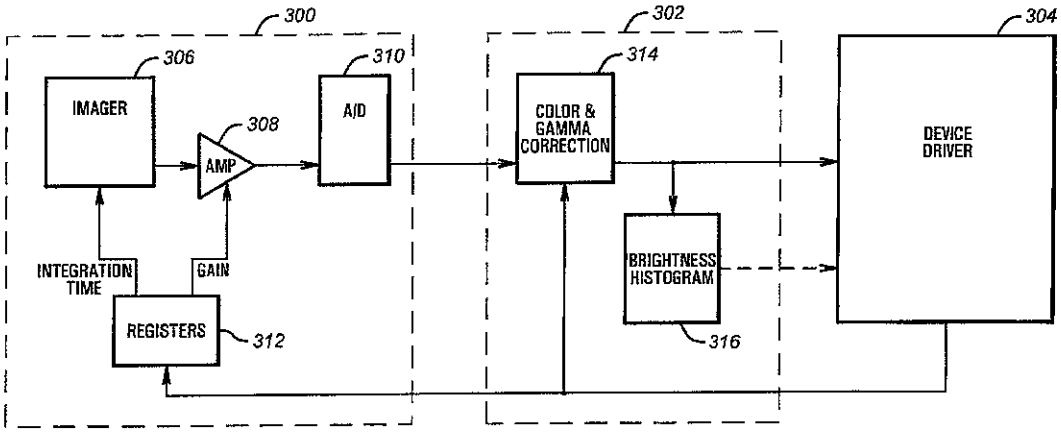
* cited by examiner

Primary Examiner—Tuan Ho
(74) *Attorney, Agent, or Firm*—Akin, Gump, Strauss, Hauer & Feld, L.L.P.

(57) **ABSTRACT**

An imager reduces lighting induced flicker by setting its pixel integration time to an integral multiple of the periods between peak intensity of the lighting. In one implementation, flicker is reduced in a 30 Hz frame rate camera capturing an image lighted with 50 Hz lighting by setting the integration time to approximately 10 ms, the period between lighting intensity peaks.

23 Claims, 4 Drawing Sheets



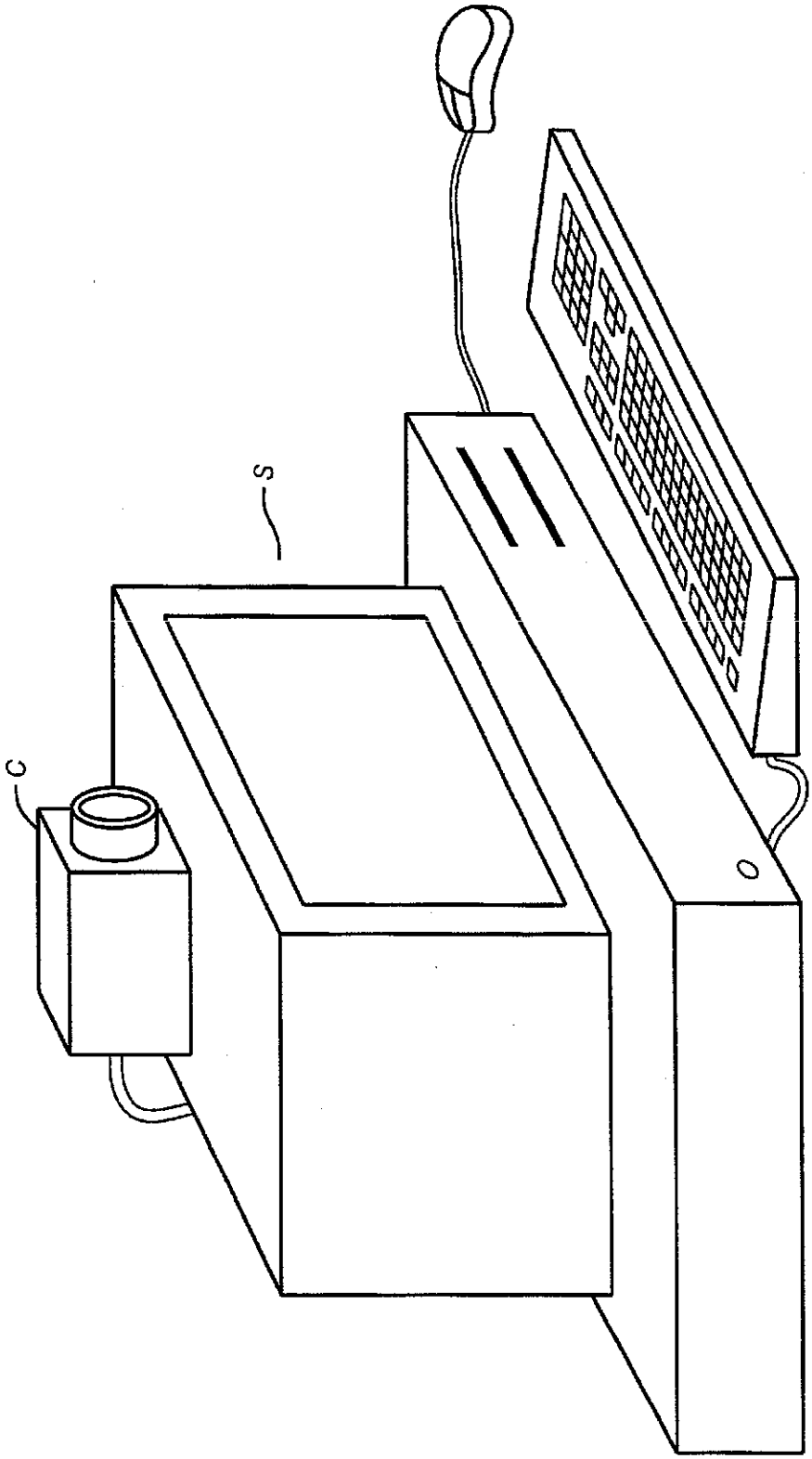


FIG. 1

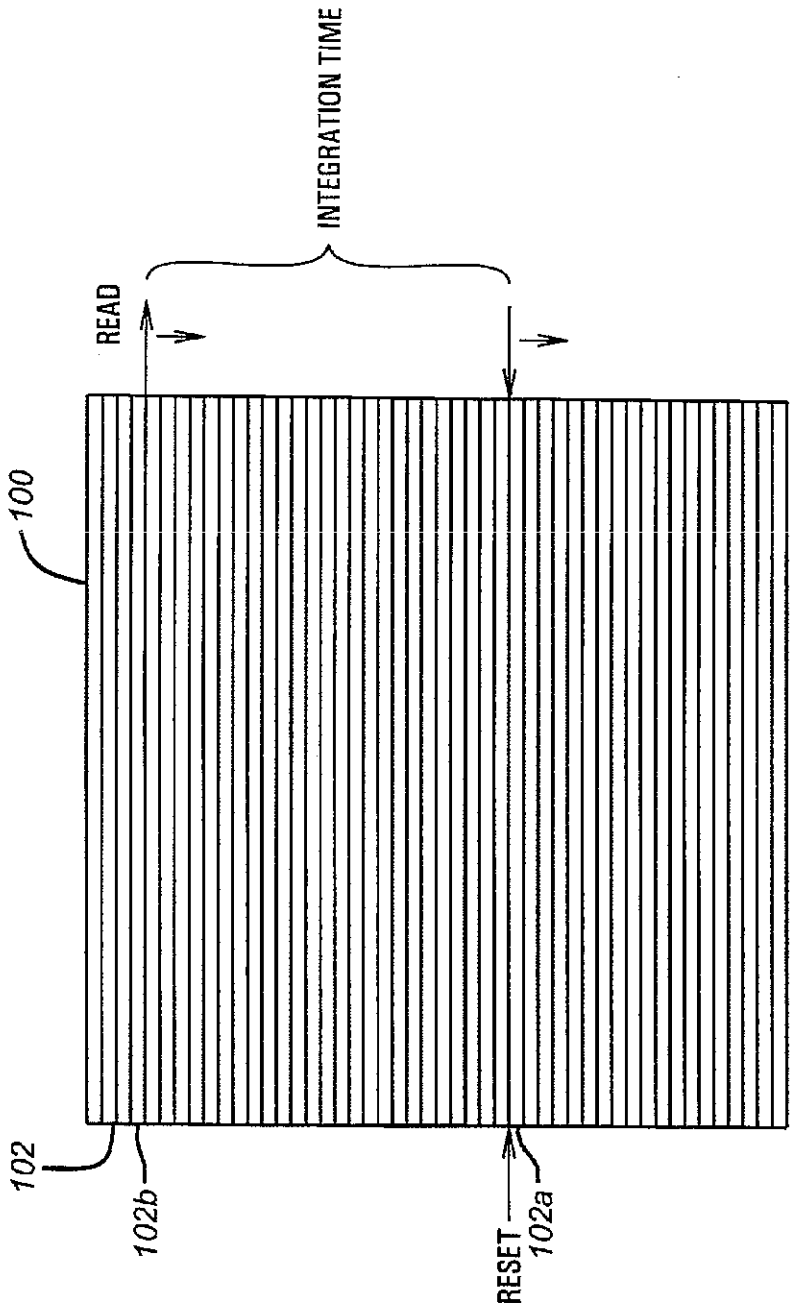


FIG. 2

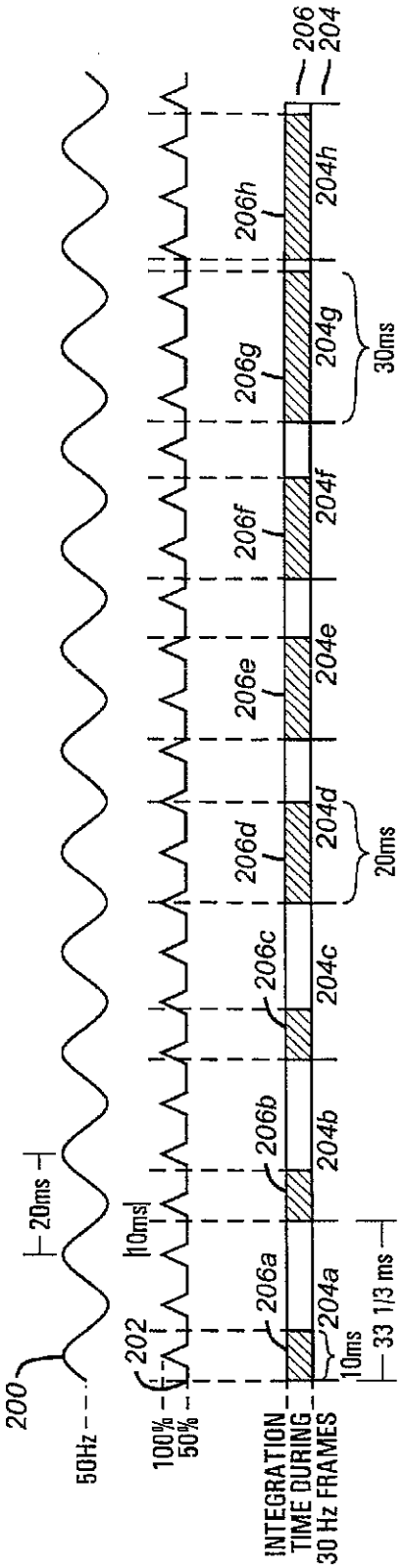

200
50Hz
20ms
10ms
202
100%
50%
206a
206b
206c
206d
206e
206f
206g
206h
206
204
204a
204b
204c
204d
204e
204f
204g
204h
10ms
33 1/3 ms
20ms
30ms
INTEGRATION TIME DURING 30 Hz FRAMES

FIG. 3A

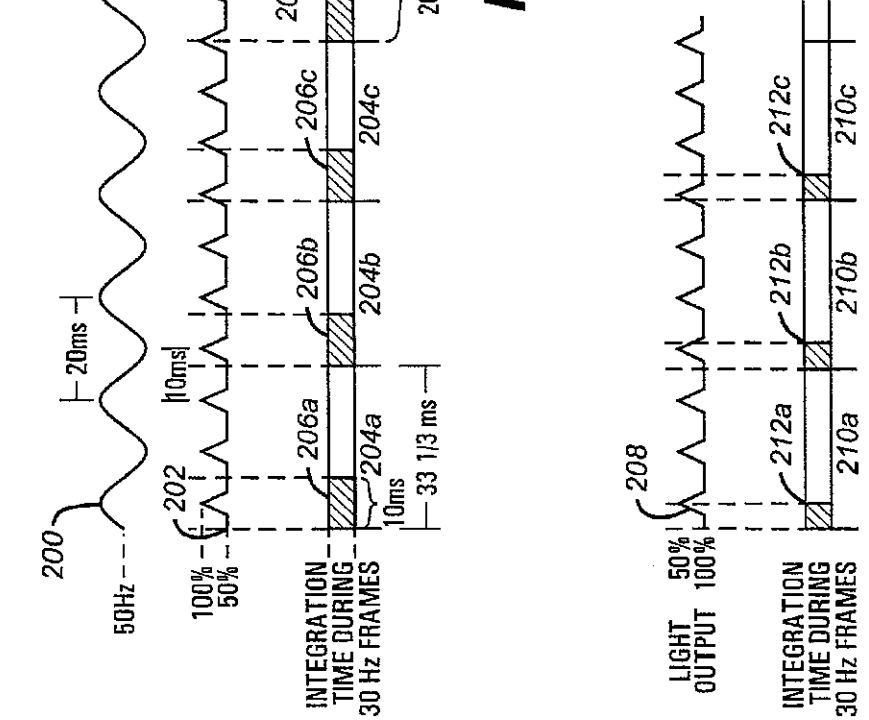

208
LIGHT OUTPUT
50%
100%
212a
212b
212c
210a
210b
210c
212
210
INTEGRATION TIME DURING 30 Hz FRAMES

FIG. 3B

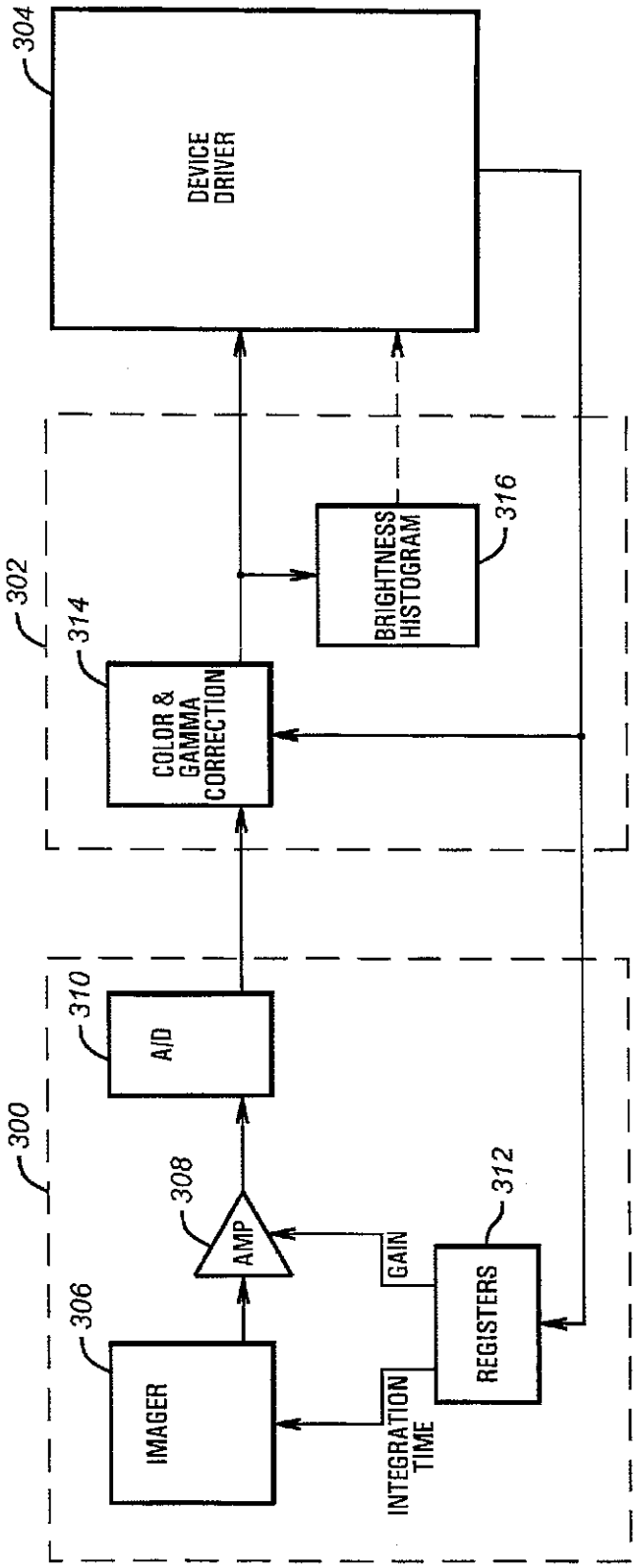

304
DEVICE DRIVER
302
316
BRIGHTNESS HISTOGRAM
314
COLOR & GAMMA CORRECTION
310
A/D
300
308
AMP
312
GAIN
REGISTERS
306
IMAGER
INTEGRATION TIME

FIG. 4

IMAGE FLICKER REDUCTION WITH FLUORESCENT LIGHTING

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention pertains to digital imaging systems, and more particularly to a digital imaging system with reduced flicker caused by fluorescent lighting.

2. Description of the Related Art

Digital imagers have become commonplace in the last decade. For both video cameras and still cameras, semiconductor devices are commonly used to capture an image on a pixel-by-pixel basis and electronically process that image. Such devices as charge coupled devices (CCDs) and CMOS digital imagers have resulted in low cost video cameras, still cameras, and more recently cameras for coupling to computer systems for video conferencing and other image capture.

One problem pertaining to imaging systems generally and to digital imagers in particular is that of flicker. Flicker can arise from many sources, but in capturing digital video flicker especially results from a relationship between some periodic phenomena and the frame rate of the camera. Digital video cameras capture images on a frame-by-frame basis, typically at a predetermined frame rate. A common frame rate in the United States and in the computer industry is 30 Hz. But when such a frame rate is used in Europe, for example, flicker can result from fluorescent lighting systems employing the standard 50 Hz alternating current power. A 50 Hz lighting system yields periodic peaks of intensity at a rate of 100 Hz, or once every 10 milliseconds. Digital imaging systems often pick up "beats" associated with this 100 Hz intensity peak being captured at a 30 Hz rate. Beats can also arise from very slight differences in fundamental frequencies such as between 69.47 Hz video and 60 Hz lighting.

A number of solutions have been employed to eliminate these "beats." These include filtering systems that filter out beat frequency, phase locking systems that attempt to lock on to the 100 Hz intensity peaks and synchronize frame capture, and a variety of other techniques.

SUMMARY OF THE INVENTION

A digital imager implementing the techniques according to the invention reduces flicker by setting an integration time for each pixel of the imager to an integral multiple of the period of lighting intensity variations. Digital imagers typically have a parameter known as integration time, which is simply the amount of time the electronic component of the pixel is allowed to capture light energy for each frame. By adjusting the integration time, the intensity of the image can be adjusted, enhancing images and preventing saturation at high intensities. In essence integration time can act as an electronic "iris." By setting the integration time to be some integral multiple of an intensity period of a lighting source, however, flicker is reduced because the amount of light captured during an integration period is independent of where the integration period starts and ends relative to the variations in lighting intensity.

In one embodiment, an imager capturing video images at 30 frames a second (for a frame period of 33⅓ milliseconds) employs an integration time that is a multiple of 10 milliseconds, the period of the peak intensities of 50 Hz lighting. Thus, the amount of light captured during each integration will be essentially the same irrespective of where in the 50 Hz fluorescent lighting cycle the integration period begins.

Further features of various embodiments of the invention include detecting the period of the peak intensity and setting the integration time accordingly, and altering the integration time as part of a system to set the overall gain of a video camera. Further, the techniques can be implemented in a variety of cameras, including a computer coupled universal serial bus camera or a stand alone video camera. In the computer coupled system, overall gain can be controlled with a software device driver.

BRIEF DESCRIPTION OF THE DRAWINGS

A better understanding of the present invention can be obtained when the following detailed description of the preferred embodiment is considered in conjunction with the following drawings, in which:

FIG. **1** is an illustration of a typical computer connected video camera implementing features according to the invention;

FIG. **2** is a diagram illustrating the concept of integration time employed by an electronic digital imager;

FIGS. **3**A and **3**B are timing diagrams illustrating how the implementation of integration time according to the invention "decouples" the light captured during integration from where within a particular lighting cycle the integration time begins; and

FIG. **4** is a block diagram of an imaging system implemented according to the invention to reduce lighting induced flicker.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENT

Turning to FIG. **1**, illustrated is a typical digital video camera C coupled to a general purpose computer system S in which features of the invention are implemented. The video camera C is preferably coupled to a computer system S via a Universal Serial Bus (USB), and together this system employs flicker reduction according to the invention. The system illustrated in FIG. **1** preferably employs a device driver on the computer system S that controls the functions of the video camera C. Further details of this system are described below in conjunction with FIG. **4**.

This system is particularly useful for videoconferencing, such as over the Internet. In particular, the video camera C preferably employs a 30 Hz image capture rate, which is compatible with the requirements of the ITU-T recommendation H.324 specification for terminals for low bit-rate multimedia communications. When a 30 Hz image capture rate is employed in the system of FIG. **1** in an environment in which 50 Hz fluorescent lighting is present, the video camera C is set to provide an integration time for each pixel of a multiple of 10 milliseconds. When the system of FIG. **1** is implemented in an environment having 60 Hz fluorescent lighting, the integration time is instead set to a multiple of 8⅓ milliseconds. These integration times correspond to the period between peaks of intensity for 50 Hz and 60 Hz fluorescent lighting respectively. Using these integration times reduces the presence of "beats" in the captured image that would otherwise arise from the relationship between the 30 Hz frame rate and the 100 Hz or 120 Hz peak intensity rate of the lighting.

The system of FIG. **1** is simply an illustrative embodiment, however, and the flicker reduction techniques according to the invention can be employed in a variety of video imaging systems other than the system of FIG. **1**.

Integration Time in a Video Imager

Digital imagers as would be used in the video camera C typically employ some technique to set each pixel's integration time, which is simply the amount of time that a pixel is allowed to gather light before that pixel is digitally read.

FIG. **2** is a diagram illustrating this concept of integration time in a video imager. Such an imager, can be, for example, a CN0352 Digital CMOS Imager by Conexant Systems, Inc. of Newport Beach, Calif. This imager provides among other things a 354×290 colorized pixel block, an on-chip 10 bit analog-to-digital converter, and an on-chip gain control. This device is typically implemented with the CN0352p Pixel Processor and Control Chip, also by Conexant Systems, Inc. This companion chip provides a variety of line-and pixel-level signal conditioning blocks as well as blocks to control the CMOS imager itself.

In FIG. **2**, illustrated is a representation of an image array **100** with a number of rows of pixels **102**. With the disclosed CN0352 imager discussed above, the image array **100** has an active pixel area of 354 rows by 290 columns. In operation, the disclosed imager employs a continuous line-by-line read of the image array **100**, although other techniques such as an interleaved read technique are possible. Prior to being read, however, the disclosed imager resets each row a predetermined period of time—the integration time—before that row is read. As illustrated in FIG. **2**, for example, a row **102***a* is reset approximately the same time a row **102***b* is read. Subsequent rows of the image array **100** are read until the row **102***a* is read an integration time period later. Thus, by adjusting how far "ahead" of a row read that row is reset, the disclosed imager adjusts the integration time.

A variety of other techniques are possible for adjusting integration time. Again the concept of integration time is simply the amount of time a particular pixel is allowed to accumulate light during a particular frame.

When the image array **100** is the CN0352 imager, each pixel consists of a photo-diode in which incoming photons are converted to electrons. During the integration time, a read transistor is switched off so that all photo generated electrons accumulate on the photo-diode's junction capacitance. The resulting sense node voltage is buffered by a second transistor that forms a source follower in combination with a current source, which is common to all pixels in each column. At the end of the integration time, the read transistor is enabled to transfer the buffered voltage to the column wire. A third transistor, the reset transistor, is then enabled to discharge the photo-signal, and the row is then read through a gain stage. The composite imager gain of the gain stage is set by a 3 bit GainControl[2:0] signal. The output of that variable gain amplifier then drives the on-chip analog to digital converter.

Each pixel includes two controls, a latch signal and a reset signal. When the reset signal goes low, the pixel starts storing charges on its junction until the latch signal goes high. At that instant, the photo voltage is transferred to variable gain amplifier and the column buffer via the composite source buffer. When the reset signal goes high to the pixel all the generated charge in the photo diode transfers through the low impedance node. In the disclosed imager, pixels are reset and latched on a row by row basis, so again as illustrated in FIG. **2**, when the row **102***a* is reset, the row **102**.*b* is being read. Then, an integration period of time later the row **102***a* is read. It will be appreciated that the integration time is a function of the frame rate and clock frequency at which the image array **100** is operated.

Matching Integration Time to Light Intensity Frequency

Turning to FIG. **3***a*, illustrated are the effects of implementing an integration time that is an integral multiple of the period of intensity of the lighting source; FIG. **36** illustrates a problem of implementing non-integral values of integration time. FIG. **3***a* illustrates a 50 Hz signal **200** used to drive a typical European fluorescent light, as well as an associated light output signal **202** of such a fluorescent light. The light output peaks during peak voltage, so the period of the peak intensity of light output is 10 milliseconds, or one-half of the 20 millisecond period of the 50 Hz signal **200**. The intensity thus peaks at a rate of 100 Hz.

In conjunction with the 50 Hz signal **200** and the light output signal **202**, shown are a sequence of frames **204** illustrating corresponding integration periods **206**. Specifically, in a first three 33⅓ millisecond frames **204***a*, **204***b* and **204***c*, shown are 10 millisecond integration times **206***a*, **206***b*, and **206***c*. Assuming, for example, the integration time is the period of time in FIG. **2** from when the row **102***b* is reset until row **102***b* is read, at the end of the integration time, the row **102***b* will be read and reset for the following frame. Comparing the integration time **206***a* to the integration time **206***c*, it is seen that the peak intensity of the light output signal **202** occurs in the middle of the integration time **206***a*, but that during the integration time **206***c* portions of two separate peaks are captured. According to the invention, however, by setting the integration time to some multiple of the ten millisecond period of the light output **202**, the amount of light captured during the integration time **206***a* is the same as the amount of light captured during the integration time **206***c* (assuming the image has not appreciably changed) because the system integrates a multiple of the period of the light output.

This is further illustrated for three subsequent frames **204***d*, **204***e*, and **204***f*, which employ 20 millisecond integration times **206***d*, **206***e*, and **206***f*. The integration period **206***d* has a peak of light output **202** falling in the middle of its period, and captures approximately half of two other peaks of light output **202**. In comparison the integration period **206***f* fully captures two complete peaks of light output **202**. But again, the amount of light captured is independent of where in the cycle of the light output **202** the integration begins.

Two succeeding frames **204***g* and **204***h* further illustrate this concept with 30 millisecond integration periods **206***g* and **206***h*, here capturing approximately three peaks of light output **202**.

This should be contrasted to the integration periods illustrated in FIG. **3***b*. FIG. **3***b* shows a light output signal **208** which corresponds to the light output signal **202**, but here, three frames **210** are illustrated with integration periods **212** that are not an integral multiple of the period of the peak intensity of light output **208**. Instead, during three frames **210***a*, **210***b*, and **210***c*, approximately 5 millisecond integration periods **212***a*, **212***b* and **212***c* is illustrated. But while the integration period **212***b* captures nearly all of the peak of light output of the signal **208**, the integration period **212***a* only captures half of that peak, thus illustrating that the amount of light captured is dependent on where the integration times begins and ends. Certain integration times can lead to a slow moving band of light on a resulting image.

Therefore, according to the invention, this flicker is reduced by providing an integration time, such as the integration time **206**, that are a multiple of the period of the peak of light output **202**.

Implementation of the Camera According to One Embodiment

Illustrated in FIG. **4** is a block diagram illustrating certain particularly useful components of a system implemented according to the invention. In FIG. **4**, an imager chip **300** is

provided in conjunction with an imager controller chip **302**, all of which communicate with a device driver **304** that would, for example, be implemented in the computer system S. In the disclosed embodiment, the imager chip **300** is the CN0352 Digital CMOS Imager and the imager controller chip **302** is the CN0352p Pixel Processor and Control Chip. The device driver **304** operates on the computer system S, but could be implemented, for example, as part of the camera C, or as part of a standalone video camera.

In the diagram of FIG. **4** a number of components have been omitted for clarity. For example, the image controller **302** generally includes a variety of signal conditioning blocks such as a noise reduction block, a synchronization block, a defective pixel correction block, a geometric scaling block, an interpolation block, a color space converter block, an edge enhancement filter, a compression block, and a USB interface.

In the disclosed embodiment, an image array **306** which corresponds to the image array **100** of FIG. **1** captures lines of video information and provides an analog signal to an amplifier **308** having a variable gain. The amplifier **308** provides an amplified analog signal an analog-to-digital converter **310**, which in the disclosed chip is a ten-bit analog to digital converter. Both the integration time of the imager **306** and the gain of the amplifier **308** are controlled by control circuitry accessed via registers **312**. The registers **312** are controlled by the imager controller chip **302**, which in turn receives a digitized image signal from the analog-to-digital converter **310**. Two blocks are illustrated the imager controller chip **302**, although as discussed above a variety of other blocks are implemented at intervening locations. In particular, a color and gamma correction block **314** ultimately receives the digitized image from the analog-to-digital converter **310**, and a brightness histogram block **316** monitors the average brightness of the digital image output from the color and gamma correction block **314**. In the disclosed embodiment, the brightness histogram block **316** actually monitors a center portion of the image and an edge portion of the image to provide two separate averages of intensity data.

The color and gamma correction block **314** then provides a corrected digital video image as output, and both that digital output and the data from the brightness histogram block **316** is ultimately received by the device driver **304** within the computer system S. Typically this data is transmitted in compressed form over a Universal Serial Bus (USB). One implementation is discussed, for example, in the USB Camera Designers Guide by Conexant Systems, Inc.

The device driver **304** is typically implemented to provide both variable brightness and automatic brightness control by adjusting portions of the imager chip **300** and the imager controller chip **302**. In the disclosed embodiment, brightness is adjusted most coarsely by setting the integration time via the registers **312**. Using a 30 Hz (or any other) frame rate with 50 Hz lighting, the integration times can be set to approximately 10 milliseconds, 20 milliseconds, or 30 milliseconds as illustrated in FIG. **3***a*. This provides three levels of intensity control, and preferably the device driver **304** sets the integration time to maximize the output of the image array **306** without oversaturating its pixels. The image from the image array **306** is then fed into the amplifier **308**, which in the disclosed embodiment provides for eight levels of amplification. This provides a finer resolution enhancement of the original three levels set by the integration time. This data is then provided to the analog-to-digital converter **310** and can be further refined by changing the gamma tables of the color and gamma correction block **314**. Thus, by using the three gain levels of integration time, the eight level of analog gain, and the multiple levels of digital gamma correction, a fine degree of brightness control can be achieved, all while maintaining the integration time at integral multiples of the period of the peak intensity of light output. The device driver **304** preferably monitors the data from the brightness histogram **316**, and over time alters the overall system gain, providing automatic gain control for the entire system.

In a typical system, the user will set the system to define the lighting frequency, or may be asked to view an image display first showing an image run at one integration time setting and then at another to determine which is best. Instead, the system could detect the country in which it is operating based on system configuration data, or, in the case of a stand alone camera, a switch setting may provide for 50 Hz versus 60 Hz lighting. A stand alone camera could directly monitor the lighting. A variety of techniques are possible.

The device driver **304** can also be placed into a setup mode to monitor "beats" within the intensity of data as provided by the brightness histogram block **316**. These beats can identify, for example, when the camera C is being implemented with 50 Hz lighting if the integration time is not set to a multiple of 10 milliseconds. For example, the integration time might be set to a multiple of 8⅓ milliseconds, the appropriate time for 60 Hz lighting, but the system may be implemented in a 50 Hz lighting system. By detecting the beats, the device driver **304** can automatically adjust the integration time via the registers **312** to a multiple of 10 milliseconds. Alternatively, the computer system can detect whether is plugged into a 50 Hz or 60 Hz power supply, and provide that information to the device driver, which would then appropriately set the integration to a multiple of 10 milliseconds or a multiple of 8⅓ milliseconds respectively.

Further, it should be understood that these techniques need not necessarily be implemented with the computer system S, but could be implemented in a standalone camera. In addition, the gain control of the device driver **304** could be implemented, for example, in a dedicated application specific integrated circuit as well in the device driver **304** of the general purpose computer systems. Similarly, although in the disclosed embodiment a particular combination of hardware and software is shown, the distribution of the various blocks among other combinations of hardware and software, or even hardware alone, is possible while implementing the features of the invention. A wide variety of configurations are available for implementing integration time set to an integral multiple of the period of peak light output. In addition, these techniques are not limited to CMOS imagers, but can be used with other types of digital imagers, for example CCD imagers, although the techniques for varying integration time may vary.

The foregoing disclosure and description of the preferred embodiment are illustrative and explanatory thereof, and various changes in the components, circuit elements, circuit configurations, and signal connections, as well as in the details of the illustrated circuitry and construction and method of operation may be made without departing from the spirit and scope of the invention.

We claim:

1. A method of reducing flicker caused by lighting having a periodic intensity using an imager having a pixel integration time, the method comprising the steps of:

setting the integration time to an integral multiple of the period of the periodic intensity of the lighting;

determining an amount to vary an overall system gain; and

adjusting the overall system gain by adjusting the integration time while maintaining the integration time at an integral multiple of the period of the periodic intensity.

2. The method of claim **1** wherein the lighting is 50 Hz lighting and wherein the setting step further comprises the step of adjusting the integration to an integral multiple of 10 ms.

3. The method of claim **2**, wherein the imager has a frame period and wherein the frame period is a non-integral multiple of the integration time.

4. The method of claim **3**, wherein the frame period is 33⅓ ms.

5. The method of claim **1**, wherein the lighting is 60 Hz lighting, and wherein the period of the periodic intensity of the lighting is 8⅓ ms.

6. The method of claim **1**, further comprising the step of:

detecting the period of the periodic intensity.

7. The method of claim **6**, wherein the detecting step further comprises:

detecting power line frequency; and

determining the period of the periodic intensity to be ½ of the period of the power line frequency.

8. The method of claim **6**, wherein the detecting step further comprises:

monitoring an output of the imager for beats of intensity; and

determining the period of the periodic intensity based on the period of the beats and the integration time.

9. The method of claim **1**, wherein the steps of determining and adjusting are performed by a software device driver in a general purpose computer.

10. The imager of claim **9**, wherein the lighting is 50 Hz lighting and wherein the integration time adjustment block adjusts the integration time to an integral multiple of 10 ms.

11. The imager of claim **10**, wherein the imager provides analog data at a frame period, and wherein the frame period is a non-integral multiple of the integration time.

12. The imager of claim **11**, wherein the frame period is 33⅓ ms.

13. The imager of claim **9**, wherein the lighting is 60 Hz lighting and wherein the integration time adjustment block adjusts the integration time to an integral multiple of 8⅓ ms.

14. An imager for a digital camera with reduced flicker caused by lighting having a periodic intensity, the imager providing data for a plurality of pixels, the imager comprising:

programmable integration time circuitry that controls an integration time of the plurality of pixels;

an integration time adjustment block coupled to the programmable integration time circuitry, the integration time adjustment block setting the integration time to an integral multiple of the period of the periodic intensity of the lighting; and

an overall gain control block that adjusts an overall system gain by adjusting the integration time while maintaining the integration time at an integral multiple of the period of the periodic intensity.

15. The imager of claim **14**, wherein the integration time adjustment block is within a software device driver in a general purpose computer.

16. The imager of claim **14**, wherein the integration time adjustment block is in an application specific integrated circuit.

17. The imager of claim **14**, further comprising:

an analog, variable gain stage receiving the data for the plurality of pixels and providing amplified analog pixel data;

an analog to digital converter receiving the amplified analog pixel data and providing digitized pixel data; and

a gamma correction stage receiving the digitized pixel data, and providing scaled pixel data.

18. The imager of claim **17**,

the overall gain control block further adjusting the overall system gain by adjusting the variable gain stage and the gamma correction block.

19. The imager of claim **18** wherein the overall gain control block adjusts overall camera gain in response to average image intensity of the scaled pixel data.

20. The imager of claim **19**, wherein the overall gain control block is implemented in a software device driver.

21. An imager providing data for a plurality of pixels for a digital camera with reduced flicker caused by lighting having a periodic intensity, the imager comprising:

means for controlling an integration time of the plurality of pixels to an integral multiple of the period of the periodic intensity of the lighting; and

means for varying an overall system gain by adjusting the integration time while maintaining the integration time at an integral multiple of the period of the periodic intensity of the lighting.

22. The imager of claim **21**, further comprising:

means for amplifying the data for the plurality of pixels, providing an amplified pixel data;

means for gamma-correcting the amplified pixel data,

wherein the means for varying an overall system gain further varies the system gain by adjusting the means for amplifying the data for the plurality of pixels and by adjusting the means for gamma-correcting the amplified pixel data.

23. The imager of claim **21**, the means for amplifying the data for the plurality of pixels comprising:

means for analog amplifying the data for the plurality of pixels, providing an amplified analog pixel data; and

means for digitally converting the amplified analog pixel data into the amplified pixel data.

* * * * *

EXHIBIT B

US006838651B1

(12) **United States Patent**
Mann

(10) **Patent No.: US 6,838,651 B1**
(45) **Date of Patent: Jan. 4, 2005**

(54) **HIGH SENSITIVITY SNAP SHOT CMOS IMAGE SENSOR**

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(73) Assignee: **ESS Technology, Inc.**, Fremont, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/113,545**

(22) Filed: **Mar. 28, 2002**

(51) **Int. Cl.**[7] **H01L 27/00**
(52) **U.S. Cl.** ..... **250/208.1**; 250/214 DC; 250/226
(58) **Field of Search** ..... 250/208.1, 214 DC, 250/226, 214 R; 356/416, 419; 341/155; 348/272, 294, 273, 280, 266; 358/474, 482

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Primary Examiner—Thanh X. Luu
Assistant Examiner—Seung C. Sohn

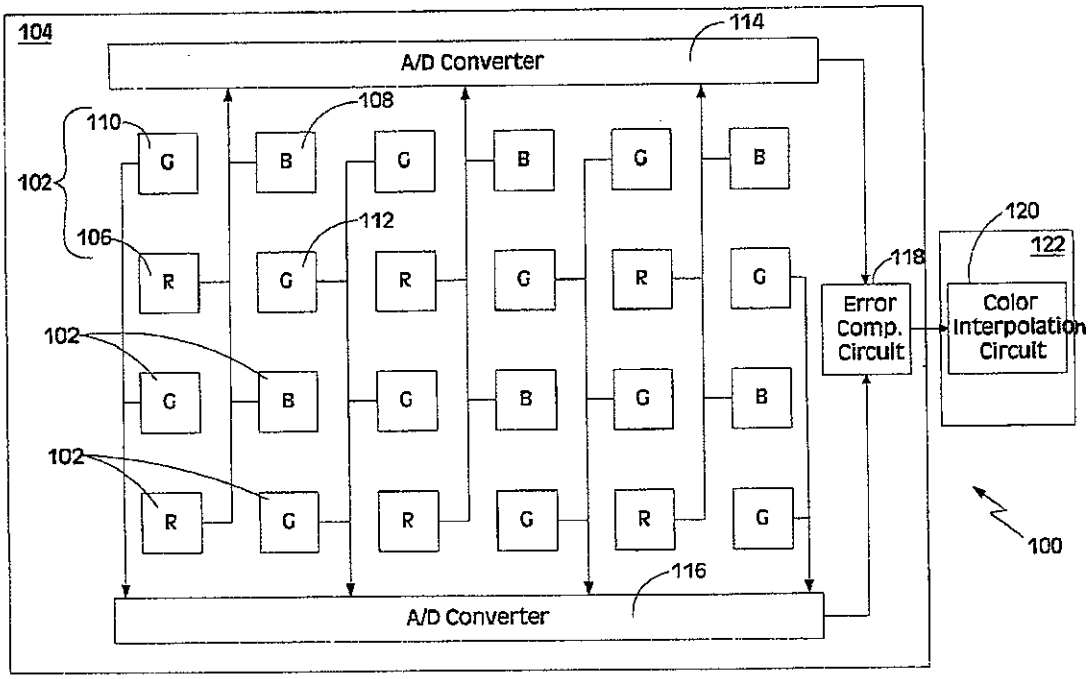
(74) *Attorney, Agent, or Firm*—Farjami & Farjami LLP

(57) **ABSTRACT**

The present invention is directed to a solid state imaging device comprising a red pixel, a blue pixel, a first green pixel, a second green pixel, two analog-to-digital converters and a color interpolation circuit. The first analog-to-digital converter converts the output of the red pixel and output of the blue pixel into digital signals. The second analog-to-digital converter converts the output of the first green pixel and output of the second green pixel into digital signals. The color interpolation circuit combines the digital signals to determine the color of the pixel.

The solid state imaging device may further comprise a third analog-to-digital converter, a fourth analog-to-digital converter, a programmable clock generator and a control. The third analog-to-digital converter converts the output of the blue pixel into a digital signal and the fourth analog-to-digital converter converts the output of the second green pixel into a digital signal. The programmable clock generator has a first clock frequency and a second clock frequency, where the first clock frequency is slower than the second clock frequency. The control is coupled to the programmable clock generator, the third analog-to-digital converter and the fourth analog-to-digital converter. The control deactivates the third and fourth analog-to-digital converters if the programmable clock generator is at the first clock frequency, and the control activates the third and fourth analog-to-digital converters if the programmable clock generator is at the second clock frequency.

22 Claims, 3 Drawing Sheets



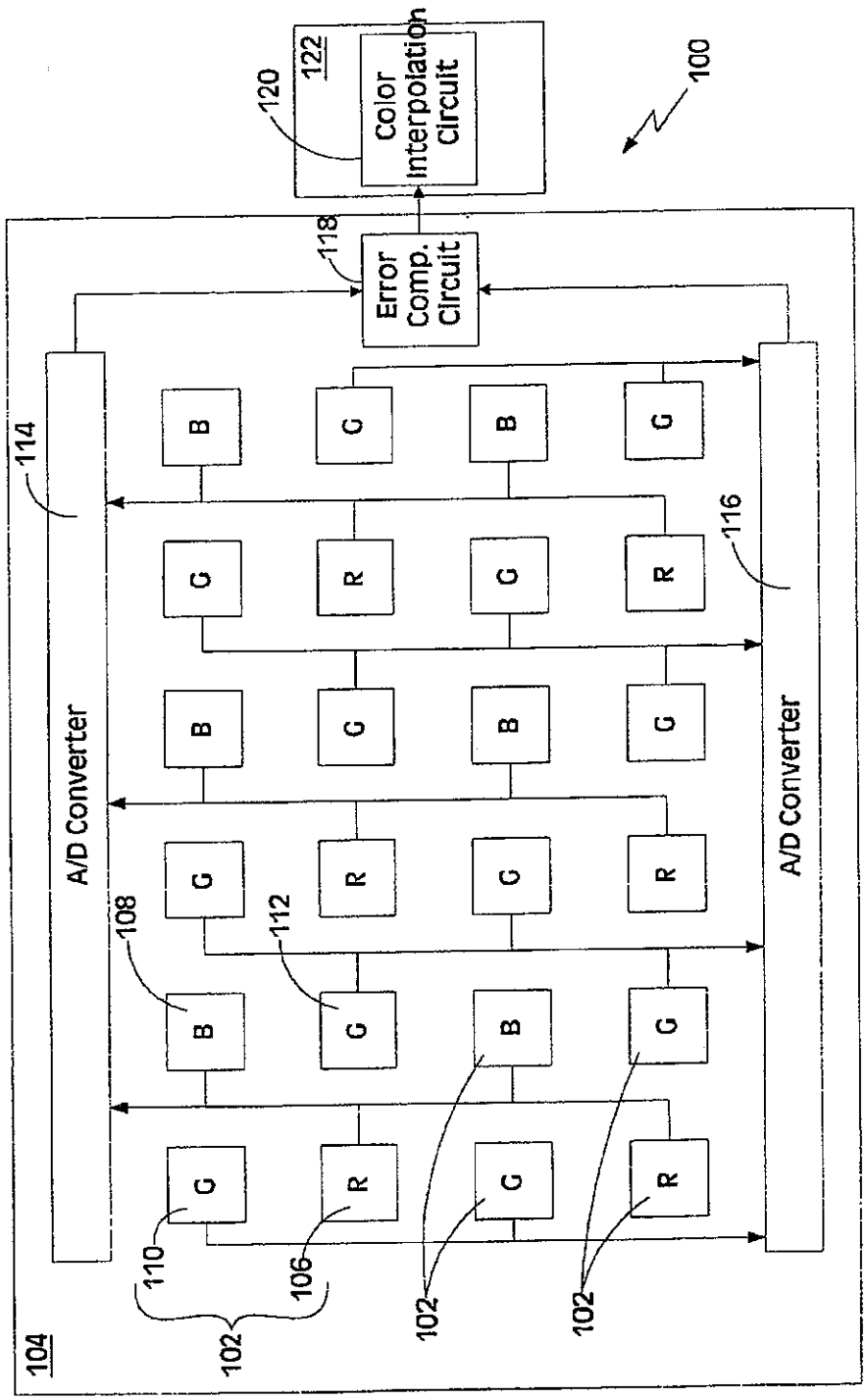

100
120
122
Color Interpolation Circuit
118
Error Comp. Circuit
114
A/D Converter
116
A/D Converter
104
108
112
110
106
102
102
102
B
G
R

FIG. 1

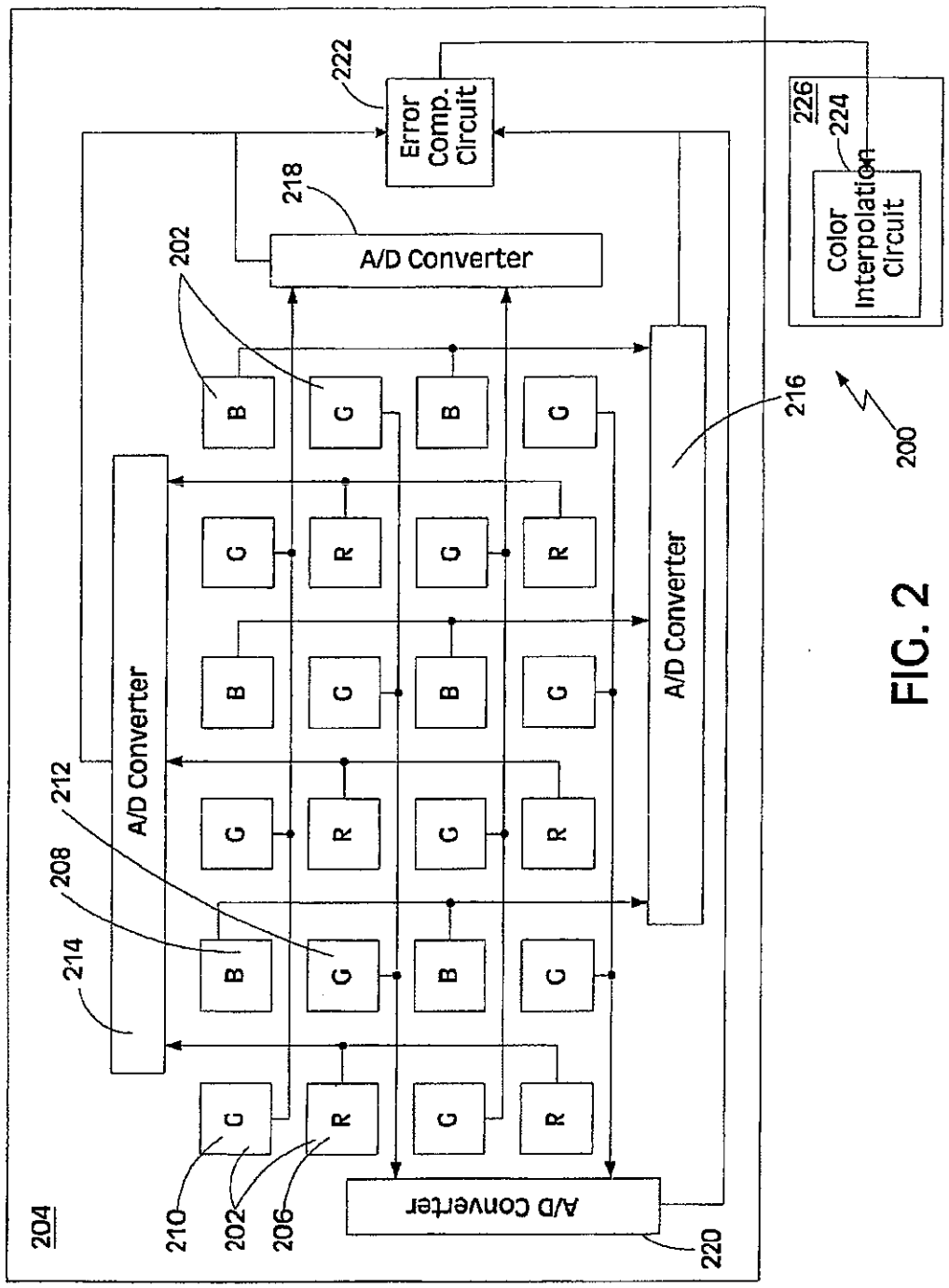

222
Error Comp. Circuit
226
224
Color Interpolation Circuit
218
A/D Converter
202
216
200
A/D Converter
A/D Converter
212
208
214
A/D Converter
204
210
202
206
220
B
G
R

FIG. 2

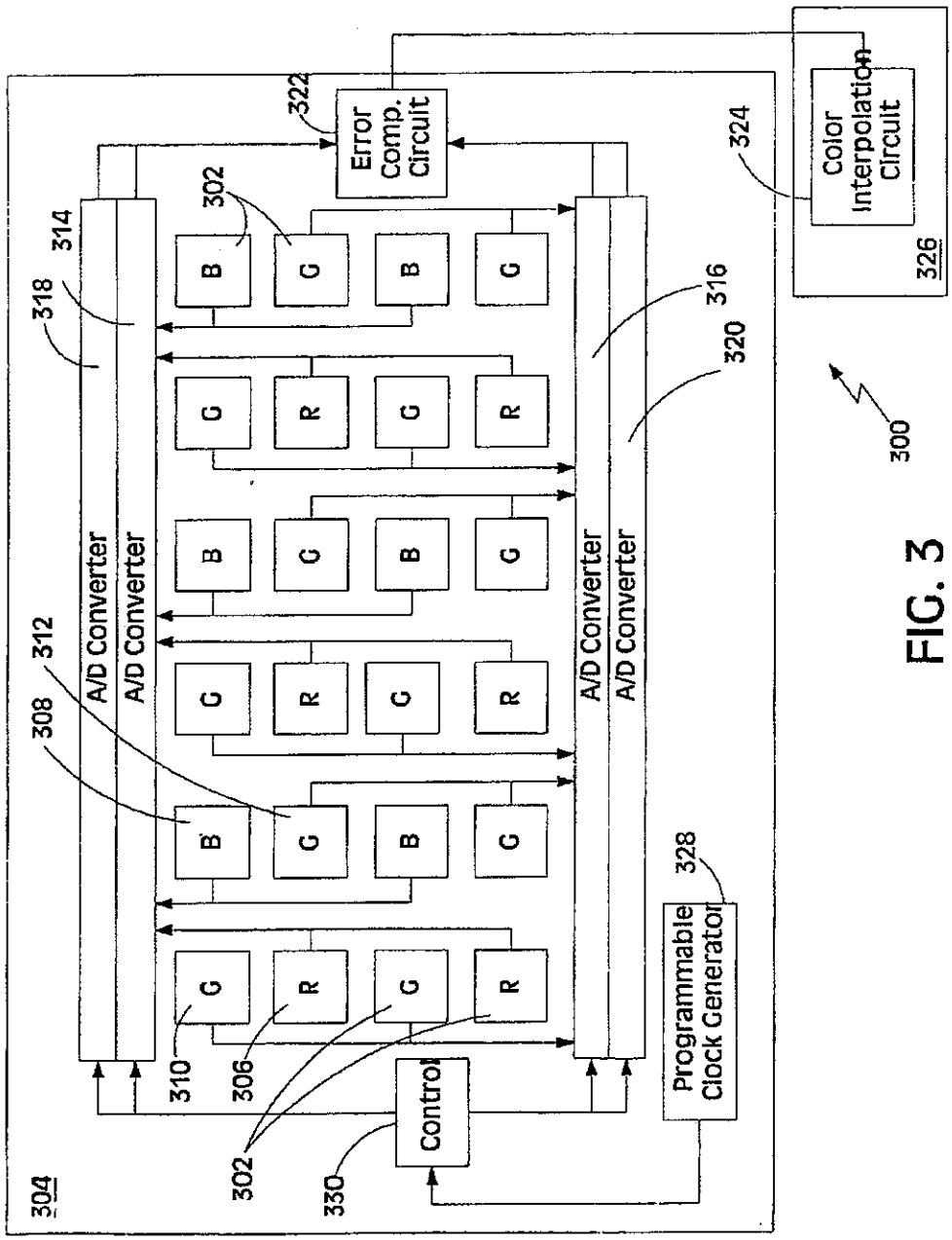

322
Error Comp. Circuit
324
Color Interpolation Circuit
326
300
302
314
318
316
320
A/D Converter
A/D Converter
A/D Converter
A/D Converter
312
308
328
Programmable Clock Generator
Control
310
306
302
330
304
B
G
R

FIG. 3

HIGH SENSITIVITY SNAP SHOT CMOS IMAGE SENSOR

TECHNICAL FIELD

This invention relates generally to solid-state imaging devices such as Complementary Metal Oxide Semiconductor ("CMOS") solid-state imagers. More particularly the invention relates to a solid-state imaging device implementing multiple analog-to-digital ("A/D") converters to obtain high frame rates.

BACKGROUND OF THE INVENTION

Solid-state image sensors (also known as "image sensors," "imagers," or "solid-state imagers") have broad applications in many areas including commercial, consumer, industrial, medical, defense and scientific fields. Solid-state image sensors convert a received image such as from an object into a signal indicative of the received image. Examples of solid-state image sensors including charge coupled devices ("CCD"), photodiode arrays, charge injection devices ("CID"), hybrid focal plane arrays and complementary metal oxide semiconductor ("CMOS") imaging devices.

Solid-state image sensors are fabricated from semiconductor materials (such as silicon or gallium arsenide) and include imaging arrays of light detecting (i.e., photosensitive) elements (also known as photodetectors) interconnected to generate analog signals representative of an image illuminating the device. These imaging arrays are typically formed from rows and columns of photodetectors (such as photodiodes, photoconductors, photocapacitors or photogates), each of which generate photo-charges. The photo-charges are the result of photons striking the surface of the semiconductor material of the photodetector, which generate free charge carriers (electron-hole pairs) in an amount linearly proportional to the incident photon radiation.

Each photodetector in the imaging array receives a portion of the light reflected from the object received at the solid-state image sensor. Each portion is known as a picture element or "pixel." Each individual pixel provides an output signal corresponding to the radiation intensity falling upon its detecting area (also known as the photosensitive or detector area) defined by the physical dimensions of the photodetector. The photo-charges from each pixel are converted to a signal (charge signal) or an electrical potential representative of the energy level reflected from a respective portion of the object. The resulting signal or potential is read and processed by video processing circuitry to create an electrical representation of the image. This signal may be utilized, for example, to display a corresponding image on a monitor or otherwise used to provide information about the optical image.

CCDs are commonly utilized as solid-state image sensors. However, CMOS technology has made significant strides in competing with CCD technology as the solid-state image sensor of choice for use in various applications such as stand-alone digital cameras and digital cameras embedded in other imaging devices (e.g., cellular phones and personal digital assistants). The principal advantages of CMOS technology are lower power consumption, higher levels of system integration that enable the creation of "camera-on-a-chip" capabilities, the ability to support very high data rates and the ease of manufacturing through the utilization of standard CMOS wafer fabrication facilities.

In video systems, CMOS technology is capable of higher frame rates than CCD technology at the same or lower levels of circuit noise because many of the elements can be designed to operate in parallel. In CCD circuits, a single amplifier transforms the received charge to voltage and supports the total data rate of the solid-state image sensor's frame rate. In CCD solid-state image sensors, the amplifier noise generally becomes dominant when 30 frames per second (FPS) is employed for image sizes over several hundred thousand pixels.

CMOS solid-state image sensors, on the other hand, utilize multiple amplifiers that allow a longer settling time between applications and higher frame rate while maintaining excellent noise rejection. In addition, CMOS solid-state image sensors may easily be equipped with a precision analog-to-digital ("A/D") converter on the solid-state image sensor chip.

In many imaging applications, it is often desirable to take a snap shot of a video image (i.e., to obtain a still image). Unfortunately, because video images are not generally of the highest quality, the snap shot of the still image will also not be of the highest quality. Such snap shots are especially inferior when compared with typical still images generated in accordance with any one of a number of still image techniques or standards generally known in the art. Typically, these higher quality still images are generated utilizing specialized image generation software.

Generally, conventional CCD solid-state imager sensors provide snap shot capability through an interline transfer approach. In the interline transfer approach, when a short exposure is required to freeze the action, the charge is transferred from the light collection junction to a junction shielded from light. The information regarding the light level is then stored on a storage node in the dark until the frame can be read. This method typically reduces motion blur and allows motion to be frozen even when the time to read the entire frame is much longer than the integration time for the exposure.

Conventional CMOS solid-state image sensors have also attempted to solve this snap shot capability problem by incorporating a storage node in the cell. However, this storage node must allow the transfer of the charge from the light collection nodes to the storage nodes, which requires an additional transistor in the cell. Such active pixel sensors are often termed four-transistor cells to distinguish them from the three-transistor active pixel sensor in CMOS solid-state image sensors. Typically, the transfer of charge from the light collection node to the storage node introduces additional reset or kT/C noise unless a very specialized field effect transistor ("FET") design is used. Additionally, cross talk may cause the storage node to continue to respond to light at 10% to 20% of the response of the lighted node. Moreover, the area required to implement the storage node also reduces the area available for light collection. Generally, for small pitch solid-state image sensor cells, the installation of a storage node reduces the available area for light collection by about 30% to 50%. The combined effects of less light collection area, transfer kT/C noise and cross talk may cause the four-transistor cell to have a signal-to-noise performance that is about ⅓ that of a conventional three-transistor cell of the same pitch. Therefore, there is a need for a high performance solid-state image sensor that solves the snap shot capability problem.

SUMMARY

A number of technical advances are achieved in the art by combining multiple A/D converters in a single CMOS

imager camera chip to attain very high frame rates. There are four color channels (one red, one blue and two greens) used to define a color image based upon the Bayer Pattern of color filters. Since each of the color signals must receive an independent gain and offset adjustment as part of the image color reconstruction, it is natural to use a separate A/D converter for each of the color channels. In the alternative, two A/D converters may be employed, where one A/D converter is used for the red and blue channels and the second A/D converter is used for the green channels. In this manner, there is no addition to the fixed pattern noise of the imager that would arise from mismatch or offset in the two A/D converters.

A CMOS imager system with a variable frame rate can be employed to accommodate very high frame rates (>60 FPS) for digital still applications to freeze motion, and lower frame rates (~30 FPS) for viewfinder or motion picture application. The variable frame rate saves power during continuous operation as the high frame rate for digital still application is employed only during the capture of a still picture at high shutter speed. Preferably, the variable frame rate is controlled by a programmable clock frequency for the imager core. When the frame rate is low, the imager core is clocked more slowly. As the frame rate is increased, a higher clock rate is applied to the imager core. For power savings, only two of the four analog-to-digital converters will be selected for low frame rates. When a high frame rate is selected, the additional analog-to-digital converters will be powered.

For example, a solid state imaging device of the present invention comprises a red pixel, a blue pixel, a first green pixel, a second green pixel, two analog-to-digital converters and a color interpolation circuit. The first analog-to-digital converter converts the outputs of the red pixel and the blue pixel into digital signals. The second analog-to-digital converter converts the outputs of the first green pixel and the second green pixel into digital signals. The color interpolation circuit combines the digital signals.

The solid state imaging device may further comprise a third analog-to-digital converter, a fourth analog-to-digital converter, a programmable clock generator and a control. The third analog-to-digital converter converts the output of the blue pixel into a digital signal and the fourth analog-to-digital converter converts the output of the second green pixel into a digital signal. The programmable clock generator has a first clock frequency and a second clock frequency, where the first clock frequency is slower than the second clock frequency. The control is coupled to the programmable clock generator, the third analog-to-digital converter and the fourth analog-to-digital converter. The control deactivates the third and fourth analog-to-digital converters if the programmable clock generator is at the first clock frequency, and the control activates the third and fourth analog-to-digital converters if the programmable clock generator is at the second clock frequency.

In another example, a solid state imaging device of the present invention comprises a red pixel, a blue pixel, a first green pixel, a second green pixel, four analog-to-digital converters and a color interpolation circuit. The first analog-to-digital converter converts the output of the red pixel into a digital signal. The second analog-to-digital converter converts the output of the blue pixel into a digital signal. The third analog-to-digital converter converts the output of the first green pixel into a digital signal. The fourth analog-to-digital converter converts the output of the second green pixel into a digital signal. The color interpolation circuit combines the four digital signals.

Other systems, methods, features and advantages of the invention will be or will become apparent to one with skill in the art upon examination of the following figures and detailed description. It is intended that all such additional systems, methods, features and advantages be included within this description, be within the scope of the invention, and be protected by the accompanying claims.

BRIEF DESCRIPTION OF THE FIGURES

The invention can be better understood with reference to the following figures. The components in the figures are not necessarily to scale, emphasis instead being placed upon illustrating the principals of the invention. Moreover, in the figures, like reference numerals designate corresponding parts throughout the different views.

FIG. 1 illustrates a block diagram of a solid state imaging device having two analog-to-digital converters, in accordance with the present invention.

FIG. 2 illustrates a block diagram of a solid state imaging device having four analog-to-digital converters, in accordance with the present invention.

FIG. 3 illustrates a block diagram of a solid state imaging device having four analog-to-digital converters and a variable frame rate, in accordance with the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. **1** illustrates a solid state imaging device **100** in accordance with the present invention. The imaging device **100** comprises a two-dimensional array of image pixels **102** disposed on a chip **104** using four color channels (one red, one blue and two greens) to define a color image. Each pixel **102** is either a red pixel **106** having a red photodiode, a blue pixel **108** having a blue photodiode or a green pixel **110**, **112** having a green photodiode. The standard approach uses identical photodiode construction for each of the sensing elements. The green photodiode responds to green light since only green light is allowed to strike the photodiode through the filter element. In a similar manner, a preferential response is created to blue and red light.

The output of each pixel **102** is a signal proportional to the amount of light incident on the pixel **102**. Accordingly, the output of the red pixel **106** is a signal proportional to the amount of red light incident on the pixel **106**. Similarly, the output of the blue pixel **108** is a signal proportional to the amount of blue light incident on the pixel **108** and the output of the green pixels **110**, **112** is a signal proportional to the amount of green light incident on the pixels **110**, **112**.

The solid state imaging device of the present invention defines a color image based upon the Bayer pattern of color filters. In particular, the imager system comprises green pixels **110**, **112** in checkerboard pattern. Thus, the green pixels **110**, **112** exist in both odd rows (**110**) and even rows (**112**). The blue pixels **108** are shown alternating with the green pixels **110** in the odd rows, and the red pixels **106** are shown alternating with the green pixels **110** in the even rows. Alternatively, the blue pixels **108** may alternate with the green pixels **112** in the even rows and the red pixels **106** may alternate with the green pixels **110** in the odd rows.

The imaging device **100** also comprises a first analog-to-digital converter **114**, a second analog-to-digital converter **116**, an error compensating circuit **118** and a color interpolation circuit **120**. The first analog-to-digital converter **114** is disposed on the chip **104**, and converts the outputs of the red pixels **106** and the blue pixels **108** into digital signals. The

second analog-to-digital converter **116** is also disposed on the chip **104**, and converts the outputs of the green pixels **110, 112** into digital signals. The error compensation circuit **118** provides an independent gain to correct the gain for each color channel. The error compensation circuit **118** also provides an independent offset to correct the fixed pattern noise offset for each color channel. Small adjustments to the gain and offset can be self-calibrated by the imager **100** by the self-testing of black and white reference rows each time the imager **100** is powered. The correction coefficients for the pair of green A/D converters **116** can then be automatically derived and stored on chip static RAM.

Color interpolation is used to determine the amount of red, green and blue light incident on each pixel. This process averages the color outputs of appropriate neighboring pixels to approximate each pixel's unknown color data. For example, for any given blue pixel **108**, the process of color interpolation determines the green content of the pixel **108** by averaging the outputs of the green pixels **110, 112** above, below, to the left and to the right of the pixel **108**. Similarly, the red content of the pixel **108** is determined by averaging the outputs of the red pixels **106** diagonally adjacent to the pixel **108**. The color interpolation circuit **120** performs the interpolation for each pixel **102** to determine the color of the pixel **102**. The color interpolation circuit **120** may be located on a second chip **122**, as shown in FIG. **1**. Alternatively, the color interpolation circuit **120** may be located on chip **104**.

FIG. **2** illustrates a second example of a solid state imaging device **200** in accordance with the present invention. Similar to the imaging device **100** of FIG. **1**, the imaging device **200** comprises a two-dimensional array of image pixels **202** disposed on a chip **204**. Each pixel **202** is a red pixel **206**, a blue pixel **208**, or a green pixel **210, 212**. The imaging device **200** also comprises four A/D converters **214, 216, 218, 220**, an error compensation circuit **222** and a color interpolation circuit **224**. The first A/D converter **214** converts the outputs of the red pixels **206** into digital signals, the second A/D converter **216** converts the outputs of the blue pixels **208** into digital signals, the third A/D converter **218** converts the outputs of the green pixels **210** into digital signals and the fourth A/D converter **220** converts the outputs of the green pixels **212** into digital signals. The error compensation circuit **222** corrects the gain and the fixed pattern noise offset for each color channel, and the color interpolation circuit **224** performs the interpolation for each pixel **202** to determine the color of the pixel **202**. The color interpolation circuit **224** may be located on a second chip **226**, as shown in FIG. **2**. Alternatively, the color interpolation circuit **224** may be located on chip **204**.

FIG. **3** illustrates a third example of a solid state imaging device **300** in accordance with the present invention. As with the previous examples, the solid state imaging device **300** comprises a two-dimensional array of image pixels **302** disposed on a chip **304**, where each pixel **302** is either a red pixel **306**, a blue pixel **308**, or a green pixel **310, 312**. The imaging device **300** also comprises four analog-to-digital converters **314, 316, 318, 320**, an error compensation circuit **322** and a color interpolation circuit **324**. The first analog-to-digital converter **314** converts the outputs of the red pixels **306** and the blue pixels **308** into digital signals. The second analog-to-digital converter **316** converts the outputs of the first and second green pixels **310, 312** into digital signals. The third analog-to-digital converter **318** converts the outputs of the blue pixels **308** into digital signals, and the fourth analog-to-digital converter **320** converts the outputs of the second green pixels **312** into digital signals. The error compensation circuit **322** is used to correct the gain and the fixed pattern noise offset for each pixel **302**, and the color interpolation circuit **324** performs the interpolation for each pixel **302** to determine the color of the pixel **302**. The color interpolation circuit **324** may be located on a second chip **326**, as shown in FIG. **3**. Alternatively, the color interpolation circuit **324** may be located on chip **304**.

The imaging device **300** further comprises a programmable clock generator **328** and a control **330**. The programmable clock generator **328** controls the frame rate of the solid state imaging device **300**. The programmable clock generator **328** has a plurality of clock frequencies, including a first clock frequency and a second clock frequency. The first clock frequency is slower than the second clock frequency. The control **330** is coupled to the programmable clock generator **328** and the analog-to-digital converters **314, 316, 318, 320**. The control **330** deactivates the third and fourth analog-to-digital converters **318, 320** if the programmable clock generator **328** is at the first clock frequency and activates the third and fourth analog-to-digital converters **318, 320** if the programmable clock generator **328** is at the second clock frequency. In addition, the control **330** sets the first analog-to-digital converter **314** to convert only the outputs of the red pixels **306** into digital signals, and sets the second analog-to-digital converter **316** to convert only the outputs of the first green pixels **310** into digital signals when the programmable clock generator **328** is at the second clock frequency.

The imaging device **300** can be employed to accommodate a plurality of frame rates. Very high frame rates (>60 FPS) are used for digital still applications to freeze motion, and lower frame rates (~30 FPS) are used for viewfinder or motion picture application. The variable frame rate saves power during continuous operation as the high frame rate for digital still application is employed only during the capture of a still picture at high shutter speed. When the frame rate is low, the imager core is clocked more slowly. As the frame rate is increased, a higher clock rate is applied to the imager core. For power savings, only two of the four analog-to-digital converters will be selected for low frame rates. When a high frame rate is selected, the additional analog-to-digital converters will be powered.

The use of multiple amplifiers and multiple A/D converters in a CMOS imager architecture raises the possibility of increased fixed pattern noise. To minimize fixed pattern noise, it is recommended that some averaging of adjacent green pixels be applied to blur any small offset between the third and fourth A/D converters. Since the rest of the color reconstruction is done by averaging over neighboring pixels, the impact of small mismatch between A/D converters will be minimal.

For digital still applications, the low light level performance will be at least 50% better with the high frame rate approach of the present invention. When low light pictures are taken, the high-speed capability will not be employed. The improved performance comes from increased light collection area afforded by the absence of a per pixel storage element. For example, a 4.0-micron pitch CMOS imager in deep submicron design rules will have a 25% fill factor for light collection when a four-transistor pixel with an integral storage node is employed. If this same 4.0-micron pixel pitch is employed to render a 3.0-transistor pixel without a storage node, then the fill factor of the pixel is 65%. This is a 2.6× improvement in signal-to-noise at low light levels.

The conventional four-transistor approach will not work as well as the 3.0-transistor pixel without a storage node in strong illumination. In addition, cross talk of 10% to 20%

adds noise to the storage element when a conventional four-transistor cell is employed. In this instance, a high frame rate is still needed for exposures under strong illumination. Without a high frame rate, the four-transistor cell image data will be highly distorted by the cross talk from light received after the "electronic shutter is closed" but before the information can be read. Therefore, unless the cross talk can be completely suppressed, the four-transistor approach requires a high frame rate to succeed and collects only 39% of the low light signal as the new high frame rate approach.

The conventional four-transistor approach will not work as well as the high frame rate approach when working with modest light levels. With the four-transistor approach, a 2.6× longer exposure will be required just to achieve an acceptable signal-to-noise ratio. Thus, the range of situations in which sufficient light is available to freeze action is reduced compared to the high frame rate approach of the present invention.

In a 0.25 micron design rule, it is possible to have less than 10 electrons read noise while sustaining high data rates by multiplexing the per column analog circuits. To sustain a high overall frame rate, a very high speed A/D converter can be designed with up to 50 megapixel data rates. However, significantly lower power consumption can be achieved by the use of multiple A/D converters with each running at 25 to 30 megapixels per second.

Acceptable performance can be achieved by comparison to that of more commonly used cameras with a mechanical shutter. It is well accepted that for normal focal length lens (near 45 degree field of view), a minimum shutter speed for snap shot applications is about $1/60^{th}$ of a second. Acceptable results can be achieved for typical non-action subjects with shutter speeds as low as $1/30^{th}$ of a second in the very steady hands of a skilled photographer. Shutter speeds of $1/125^{th}$ of a second achieve acceptable motion capture for most casual photography. When shutter speed faster than about $1/100^{th}$ of a second are called for, the typical 35 mm camera no longer can open and close the shutter with sufficient speed. A moving slit approach is used with the width of the slit adjusted to control the exposure. This moving slit is very similar to the electronic scrolling shutter of a digital still camera. Therefore, it is safe to assume that frame rages of $1/60^{th}$ of a frame per second are adequate for low-end photography. It can also be estimated that a frame rate of $1/125^{th}$ of a second would do an excellent job (comparable to low end 35 mm camera systems) of stopping action for most camera users.

The minimum 60 frames per second can be achieved with up to about 2.0 million pixels and the application of four A/D converters. This can be accomplished without serious compromise on signal-to-noise and fixed pattern noise. The overall performance will be superior to a four-transistor design of the same pitch. Video frame rates of 30 frames per second can be achieved with four low power A/D converters for imager sized up to four million pixels. In addition, for applications such as movie making and television where power consumption is not an issue, even higher data rates and frame rates can be achieved by a CMOS approach with multiple A/D converters.

While various embodiments of the application have been described, it will be apparent to those of ordinary skill in the art that many more embodiments and implementations are possible that are within the scope of this invention. Accordingly, the invention is not to be restricted except in light of the attached claims and their equivalents.

What is claimed:

1. A solid state imaging device, comprising:

a red pixel having an output;

a blue pixel having an output;

a first green pixel having an output;

a second green pixel having an output;

a first analog-to-digital converter connected to the output of the red pixel for converting the output of the red pixel into a first digital signal and connected to the output of the blue pixel for converting the output of the blue pixel into a second digital signal;

a second analog-to-digital converter connected to the output of the first green pixel for converting the output of the first green pixel into a third digital signal and connected to the output of the second green pixel for converting the output of the second green pixel into a fourth digital signal; and

a color interpolation circuit for combining the first, second, third and fourth digital signals.

2. The solid state imaging device of claim 1, further comprising an error compensation circuit for correcting a gain of one of the output of the red pixel, the output of the blue pixel, the output of the first green pixel and the output of the second green pixel.

3. The solid state imaging device of claim 1, further comprising an error compensation circuit for correcting a fixed pattern noise offset from one of the output of the red pixel, the output of the blue pixel, the output of the first green pixel and the output of the second green pixel.

4. The solid state imaging device of claim 1 further comprising a first chip and a second chip, wherein the red pixel, the blue pixel, the first green pixel, the second green pixel, the first analog-to-digital converter and the second analog-to-digital converter are disposed on the first chip and the color interpolation circuit is disposed on the second chip.

5. The solid state imaging device of claim 1 further comprising a chip, wherein the red pixel, the blue pixel, the first green pixel, the second green pixel, the first analog-to-digital converter, the second analog-to-digital converter and the color interpolation circuit are disposed on the chip.

6. The solid state imaging device of claim 1, further comprising:

a third analog-to-digital converter connected to the output of the blue pixel for converting the output of the blue pixel into a fifth digital signal;

a fourth analog-to-digital converter connected to the output of the second green pixel for converting the output of the second green pixel into a sixth digital signal;

a programmable clock generator having a first clock frequency and a second clock frequency, wherein the first clock frequency is slower than the second clock frequency; and

a control coupled to the programmable clock generator, the first analog-to-digital converter, the second analog-to-digital converter, the third analog-to-digital converter and the fourth analog-to-digital converter,

wherein, if the programmable clock generator is at the first clock frequency, the control deactivates the third and fourth analog-to-digital converters, and sets the first analog-to-digital converter to convert the output of the blue pixel into the second digital signal and the second analog-to-digital converter to convert the output of the second green pixel into the fourth digital signal, and

wherein, if the programmable clock generator is at the second clock frequency, the control activates the third

analog-to-digital converter to convert the output of the blue pixel into the fifth digital signal and the fourth analog-to-digital converter to convert the output of the second green pixel into the sixth digital signal, and sets the first analog-to-digital converter not to convert the output of the blue pixel into the second digital signal and the second analog-to-digital converter not to convert the output of the second green pixel into the fourth digital signal.

7. The solid state imaging device of claim **6**, wherein the first analog-to-digital converter converts the output of the red pixel and the second analog-to-digital converter converts the output of the first green pixel when the programmable clock generator is at the second clock frequency.

8. The solid state imaging device of claim **6**, wherein the programmable clock generator controls a frame rate of the solid state imaging device.

9. The solid state imaging device of claim **6**, wherein the programmable clock generator comprises a plurality of clock frequencies.

10. The solid state imaging device of claim **6** further comprising a first chip and a second chip, wherein the red pixel, the blue pixel, the first green pixel, the second green pixel, the first analog-to-digital converter, the second analog-to-digital converter, the third analog-to-digital converter, the fourth analog-to-digital converter, the programmable clock generator and the control are disposed on the first chip and the color interpolation circuit is disposed on the second chip.

11. The solid state imaging device of claim **6** further comprising a chip, wherein the red pixel, the blue pixel, the first green pixel, the second green pixel, the first analog-to-digital converter, the second analog-to-digital converter, the third analog-to-digital converter, the fourth analog-to-digital converter, the programmable clock generator, the control and the color interpolation circuit are disposed on the chip.

12. The solid state imaging device of claim **6**, wherein the fifth digital signal is substantially the same as the second digital signal and the sixth digital signal is substantially the same as the fourth digital signal.

13. A solid state imaging device, comprising:

groups of pixels, wherein each of said groups of pixels include:

a red pixel having an output;

a blue pixel having an output;

a first green pixel having an output; and

a second green pixel having an output;

a first analog-to-digital converter connected to the output of the red pixel for converting the output of the red pixels into a first digital signal and connected to the output of the blue pixel for converting the output of the blue pixels into a second digital signal;

a second analog-to-digital converter connected to the output of the first green pixel for converting the output of the first green pixels into a third digital signal and connected to the output of the second green pixel for converting the output of the second green pixels into a fourth digital signal; and

a color interpolation circuit for combining the first, second, third and fourth digital signals.

14. The solid state imaging device of claim **13** further comprising a first chip and a second chip, wherein the groups of pixels, the first analog-to-digital converter and the second analog-to-digital converter are disposed on the first chip and the color interpolation circuit is disposed on the second chip.

15. The solid state imaging device of claim **13** further comprising a chip, wherein the groups of pixels, the first analog-to-digital converter, the second analog-to-digital converter and the color interpolation circuit are disposed on the chip.

16. The solid state imaging device of claim **13**, further comprising:

a third analog-to-digital converter connected to the output of the blue pixel for converting the output of the blue pixels into a fifth digital signal;

a fourth analog-to-digital converter connected to the output of the second green pixel for converting the output of the second green pixels into a sixth digital signal;

a programmable clock generator having a first clock frequency and a second clock frequency, wherein the first clock frequency is slower than the second clock frequency; and

a control coupled to the programmable clock generator, the first analog-to-digital converter, the second analog-to-digital converter, the third analog-to-digital converter and the fourth analog-to-digital converter,

wherein, if the programmable clock generator is at the first clock frequency, the control deactivates the third and fourth analog-to-digital converters, and sets the first analog-to-digital converter to convert the output of the blue pixels into the second digital signal and the second analog-to-digital converter to convert the output of the second green pixels into the fourth digital signal, and

wherein, if the programmable clock generator is at the second clock frequency, the control activates the third analog-to-digital converter to convert the output of the blue pixels into the fifth digital signal and the fourth analog-to-digital converter to convert the output of the second green pixels into the sixth digital signal, and sets the first analog-to-digital converter not to convert the output of the blue pixels into the second digital signal and the second analog-to-digital converter not to convert the output of the second green pixels into the fourth digital signal.

17. The solid state imaging device of claim **16**, wherein the fifth digital signal is substantially the same as the second digital signal and the sixth digital signal is substantially the same as the fourth digital signal.

18. An imaging method comprising:

converting an output of a red pixel into a first digital signal using a first analog-to-digital converter;

converting an output of a blue pixel into a second digital signal using the first analog-to-digital converter;

converting an output of a first green pixel into a third digital signal using a second analog-to-digital converter;

converting an output of a second green pixel into a fourth digital signal using the second analog-to-digital converter; and

combining the first, second, third and fourth digital signals using a color interpolation circuit.

19. The imaging method of claim **18** further comprising: correcting a gain of one of the output of the red pixel, the output of the blue pixel, the output of the first green pixel and the output of the second green pixel.

20. The imaging method of claim **18** further comprising: correcting a fixed pattern noise offset from one of the output of the red pixel, the output of the blue pixel, the output of the first green pixel and the output of the second green pixel.

21. The imaging method of claim **18**, wherein the red pixel, the blue pixel, the first green pixel, the second green

pixel, the first analog-to-digital converter and the second analog-to-digital converter are disposed on a first chip and the color interpolation circuit is disposed on a second chip.

22. The imaging method of claim 18, wherein the red pixel, the blue pixel, the first green pixel, the second green pixel, the first analog-to-digital converter, the second analog-to-digital converter and the color interpolation circuit are disposed on a chip.

* * * * *

EXHIBIT C

US006838715B1

(12) **United States Patent**
Bencuya et al.

(10) **Patent No.: US 6,838,715 B1**
(45) **Date of Patent: Jan. 4, 2005**

(54) **CMOS IMAGE SENSOR ARRANGEMENT WITH REDUCED PIXEL LIGHT SHADOWING**

(75) Inventors: **Selim Bencuya**, Irvine, CA (US); **Richard Mann**, Torrance, CA (US); **Erik Stauber**, San Diego, CA (US)

(73) Assignee: **ESS Technology, Inc.**, Fremont, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 25 days.

(21) Appl. No.: **10/425,488**

(22) Filed: **Apr. 29, 2003**

Related U.S. Application Data

(60) Provisional application No. 60/376,750, filed on Apr. 30, 2002.

(51) **Int. Cl.**[7] **H01L 31/062**

(52) **U.S. Cl.** **257/291**; 257/184; 257/187; 257/203; 257/292; 257/293; 257/433; 257/461; 257/462; 257/929

(58) **Field of Search** 257/184, 187, 257/203, 221, 291–293, 462, 929

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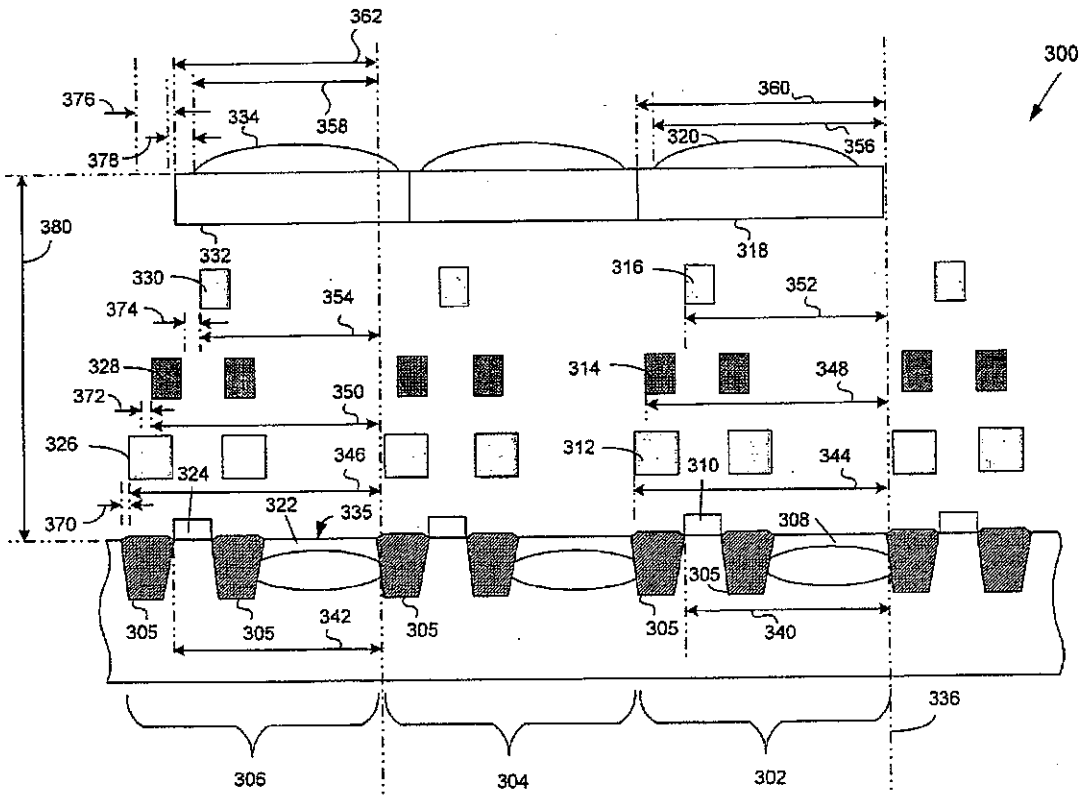
(74) *Attorney, Agent, or Firm*—Farjami & Farjami LLP

(57) **ABSTRACT**

An exemplary CMOS image sensor comprises a plurality of pixels arranged in an array. The plurality of pixels includes a first pixel proximate an optical center of the array, and a second pixel proximate a peripheral edge of the array. The CMOS image sensor further comprises a first metal interconnect segment associated with the first pixel situated in a first metal layer, and a second metal interconnect segment associated with the second pixel situated in the first metal layer. The second metal interconnect segment is shifted closer to the optical center of the array than the first metal interconnect segment so that the second metal interconnect segment approximately aligns with a principle ray angle incident the second pixel, thereby reducing pixel light shadowing.

20 Claims, 6 Drawing Sheets



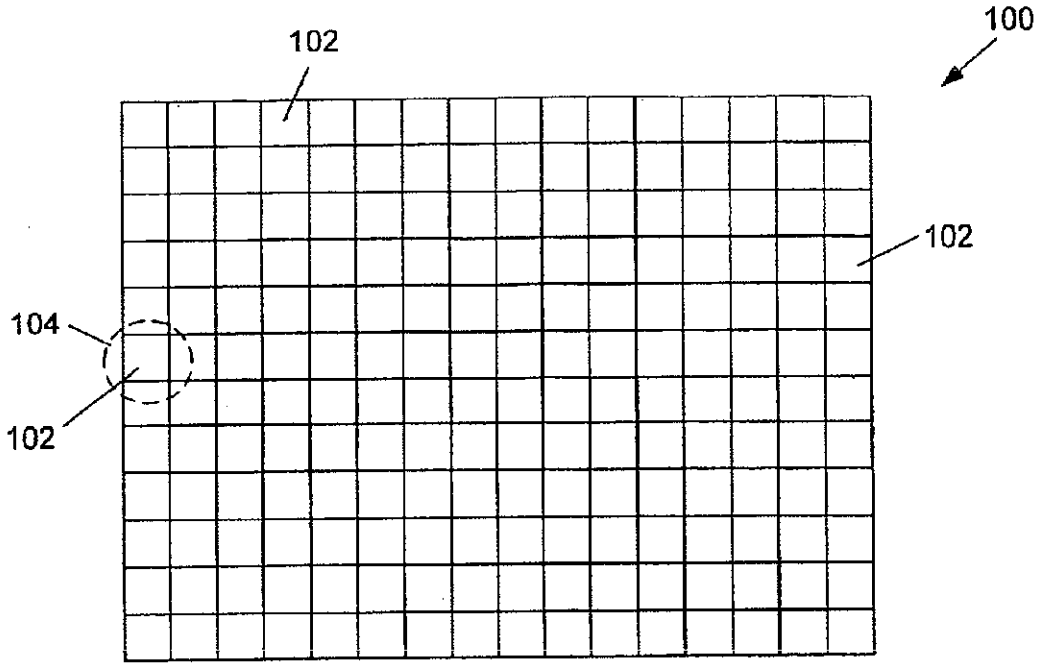


FIG. 1A

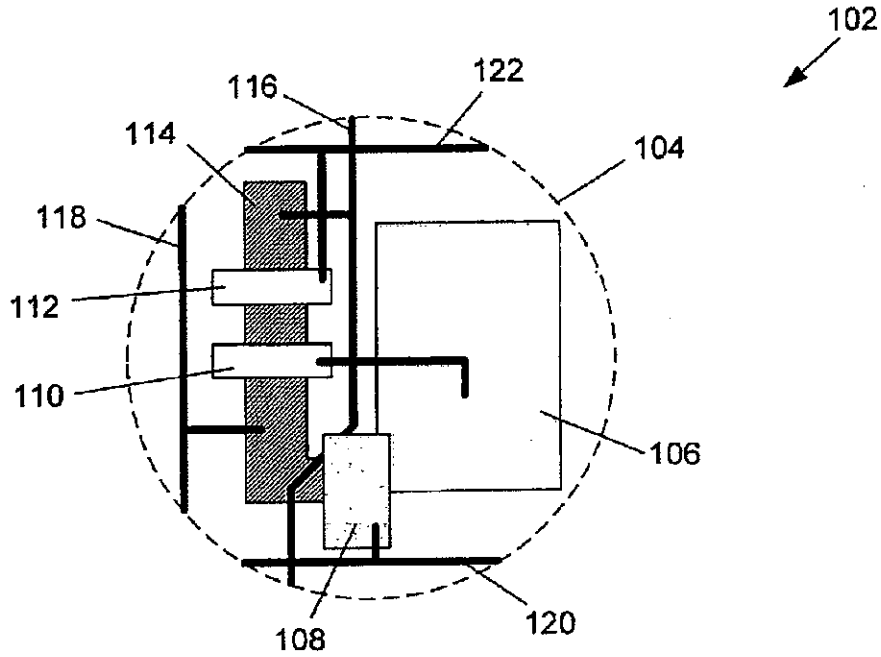


FIG. 1B

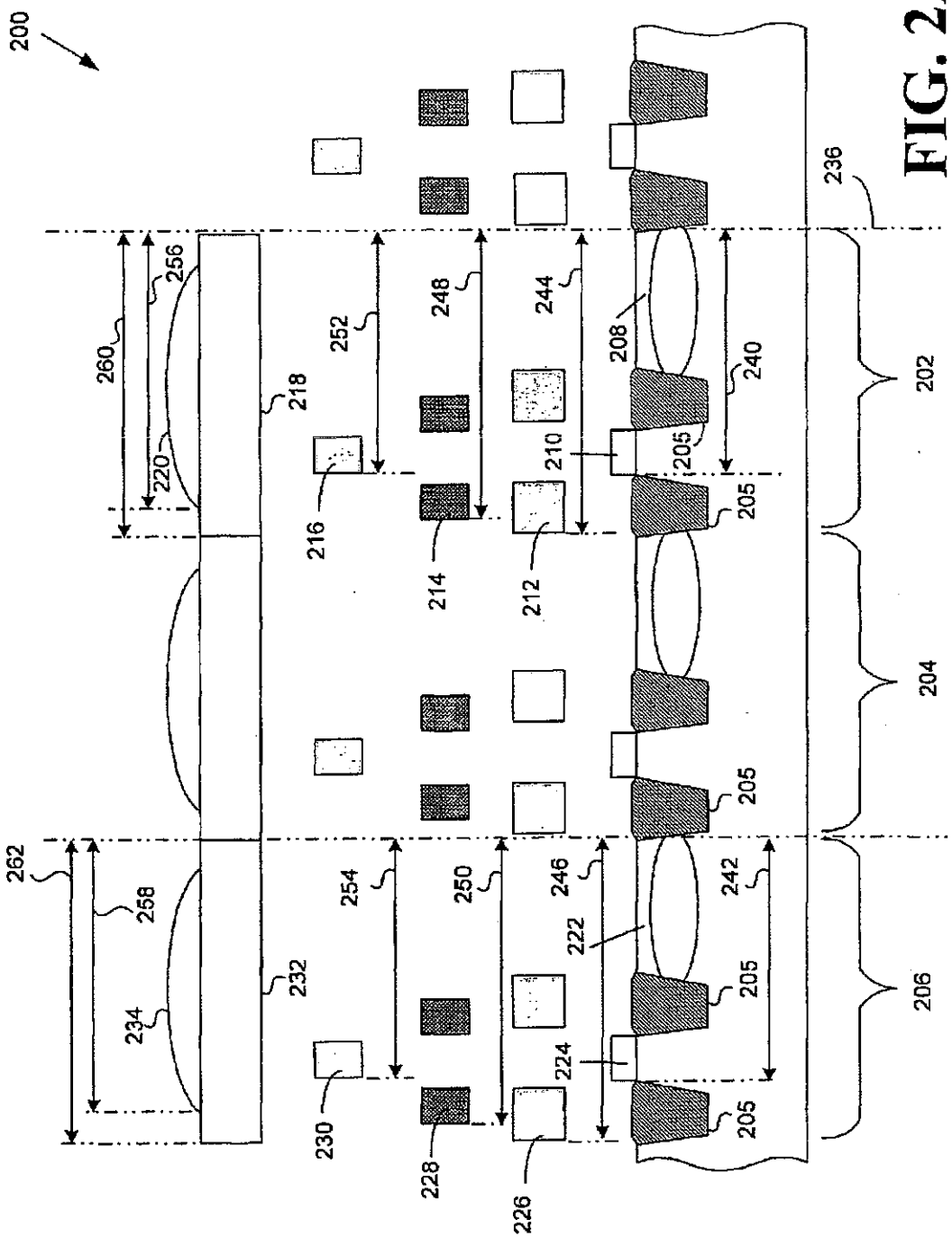

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FIG. 2A

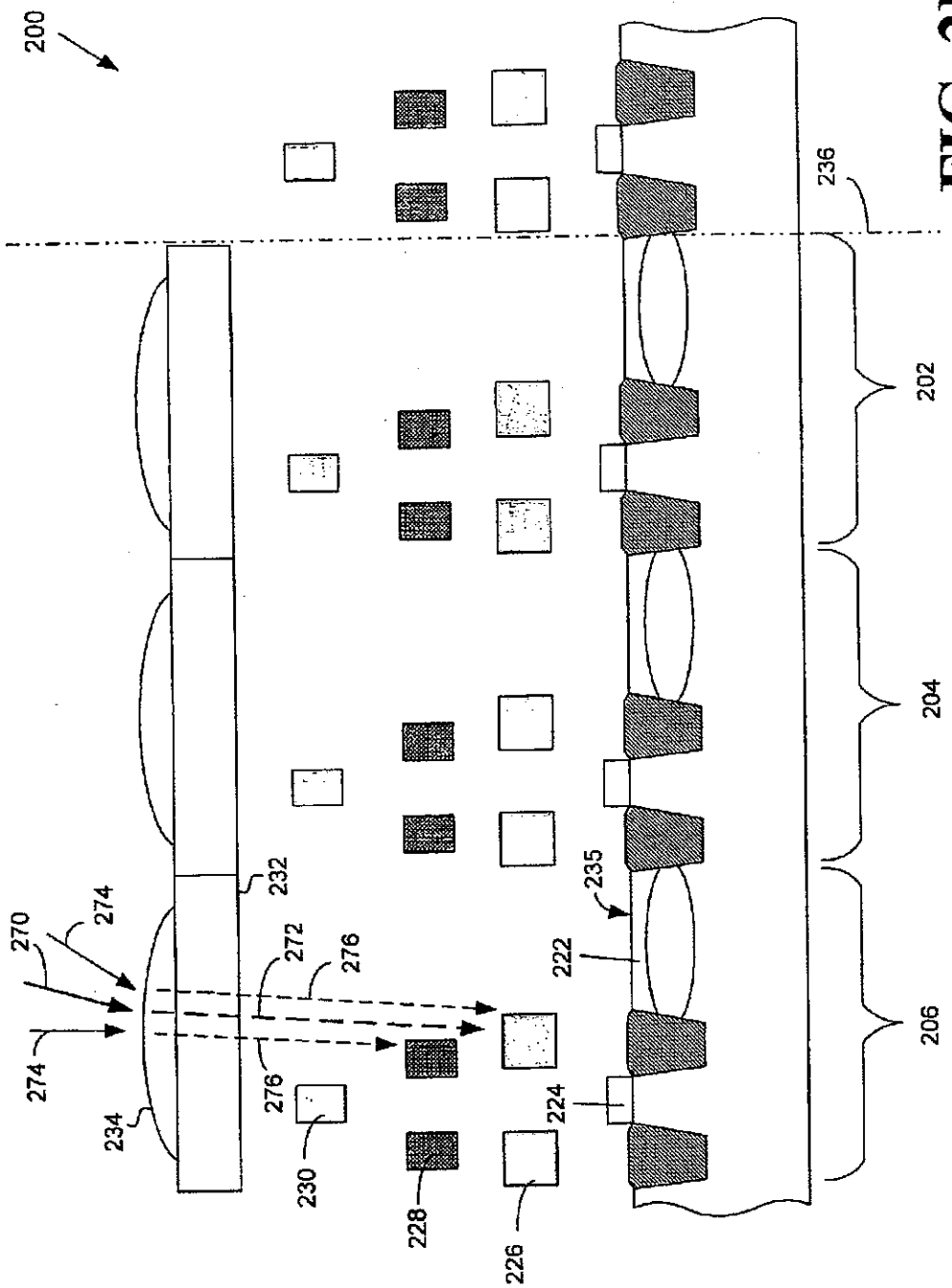
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FIG. 2B

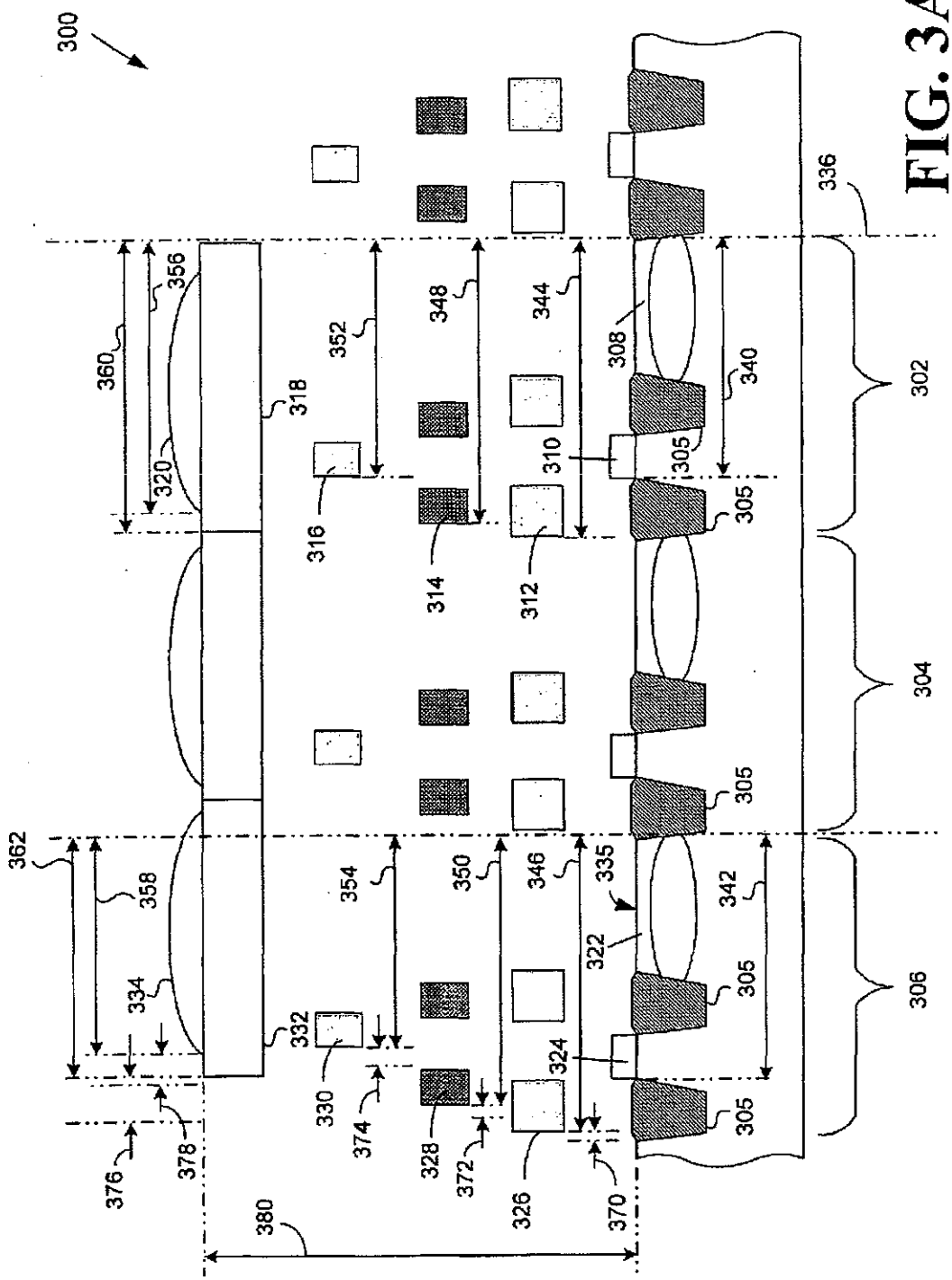
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FIG. 3A

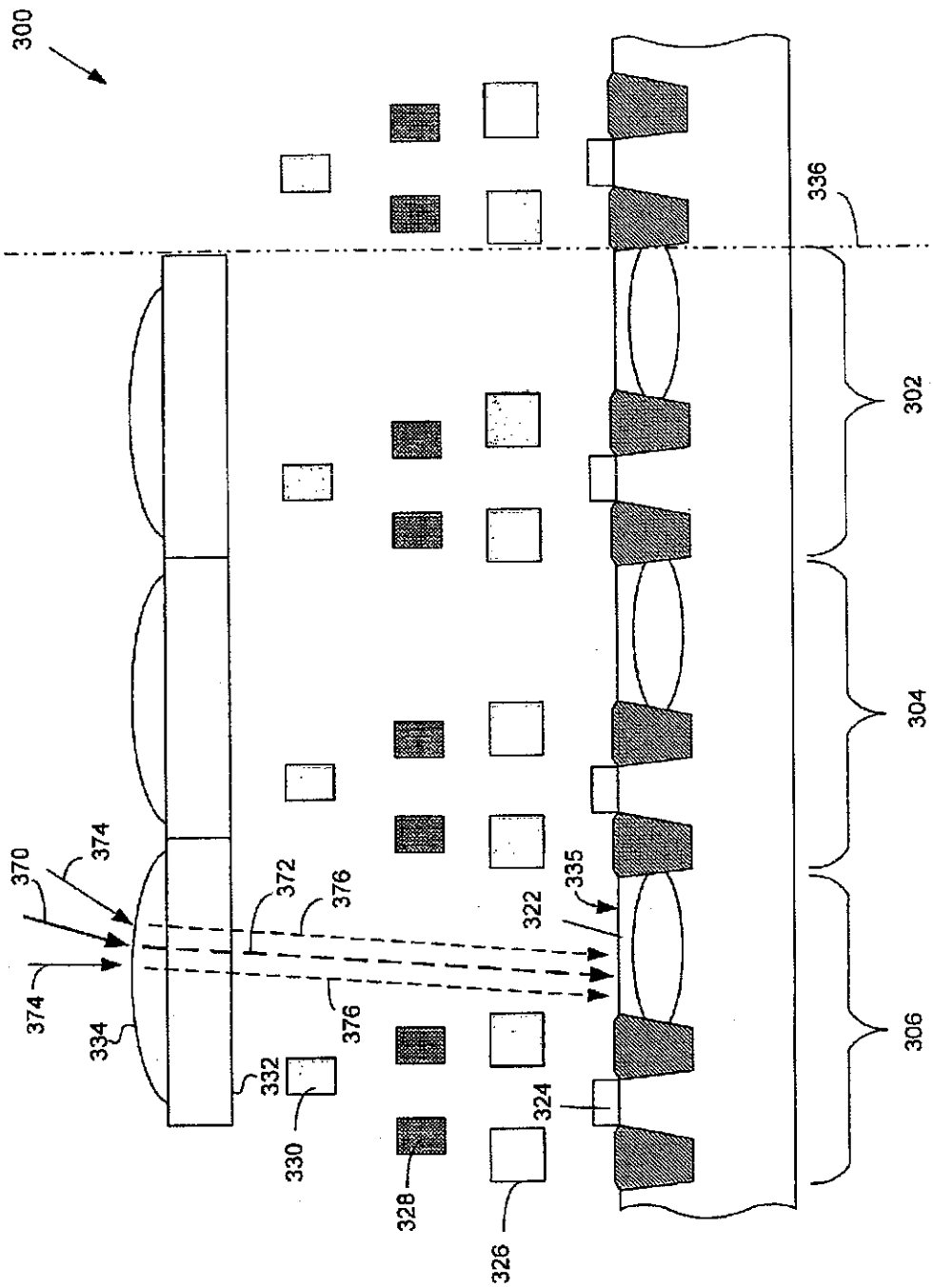
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FIG. 3B

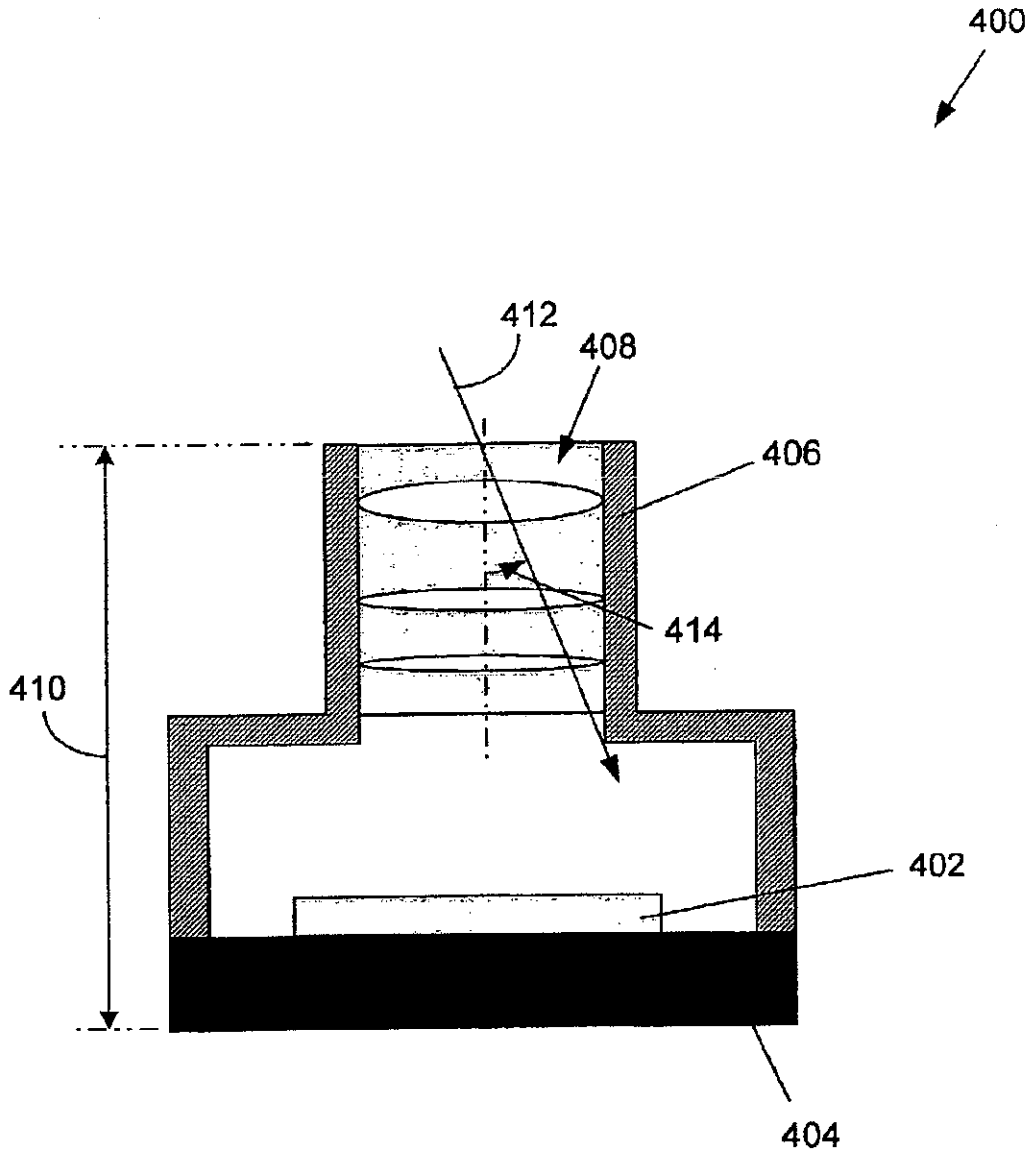

FIG. 4

CM OS IMAGE SENSOR ARRANGEMENT WITH REDUCED PIXEL LIGHT SHADOWING

RELATED APPLICATIONS

The present application claims the benefit of U.S. provisional patent application Ser. No. 60/376,750, filed on Apr. 30, 2002, the disclosure of which is hereby fully incorporated by reference in the present application.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention is generally in the field of solid state imaging devices. More specifically, the invention is in the field of Complementary Metal Oxide Semiconductor ("CMOS") imaging devices.

2. Related Art

Solid-state image sensors (also known as "solid-state imagers," "image sensors," and "imagers") have broad applications in many areas and in a number of fields. Solid-state image sensors convert a received image into a signal indicative of the received image. Examples of solid-state image sensors include charge coupled devices ("CCD"), photodiode arrays, charge injection devices ("CID"), hybrid focal plane arrays and CMOS imaging devices (also known as "CMOS image sensors" or "CMOS imaging arrays").

Solid-state image sensors are fabricated from semiconductor materials, such as silicon or gallium arsenide, and comprise imaging arrays of light detecting, i.e., photosensitive, elements (also known as "photodetectors" or "photoreceptors") interconnected to generate analog signals representative of an image illuminating the device. A typical imaging array comprises a number of photodetectors arranged into rows and columns, each photodetector generating photo-charges. The photo-charges are the result of photons striking the surface of the semiconductor material of the photodetector, and generating free charge carriers (electron-hole pairs) in an amount linearly proportional to the incident photon radiation. The photo-charges from each pixel are converted to a "charge signal" which is an electrical potential representative of the energy level reflected from a respective portion of the object and received by the solid-state image sensor. The resulting signal or potential is read and processed by video/image processing circuitry to create a signal representation of the image.

In recent years, CMOS image sensors have become a practical implementation option for imagers and provide cost and power advantages over other technologies such as CCD or CID. A conventional CMOS image sensor is typically structured as an imaging array of pixels, each pixel including a photodetector and a transistor region, and as discussed above, each pixel converts the incoming light into an electronic signal. In a typical three-transistor active pixel design for a CMOS image sensor, each pixel includes four wires (or "metal interconnect lines" or "metal interconnect segments") and three transistors, namely, a reset transistor, a source-follower transistor, and a select transistor. Two metal interconnect segments are disposed horizontally to provide row selection for either resetting the pixel or reading the pixel. Two other metal interconnect segments are disposed vertically (or substantially perpendicular to the first two metal interconnect segments) to provide column selection for both reading and resetting the pixel.

In conventional CMOS image sensors, the arrangement of the pixel's structures, including the relative positioning of the photodetector, the transistor region, and the metal interconnect segments, as well other structural elements, has presented problems. A major problem which conventional CMOS image sensors exhibit is pixel light shadowing (also referred to as "geometric shadowing"). Pixel light shadowing is caused when the average ray or principal ray striking the pixel deviates significantly from normal (or perpendicular to the imaging array plane). Under these conditions, one or more of the pixel elements situated over the photodetector may block a significant amount of light from being directed at the photodetector. As a result, the brightness of the resulting image is significantly reduced, resulting in poor image quality. Moreover, the pixels situated at the periphery of the imaging array are significantly more susceptible to pixel light shadowing. As a result, the resulting images have significant and undesirable brightness falls off at the edges of the field of view. This problem is further exacerbated due to the loss of brightness at the edge of field of view common to most lens systems due to 1/Cosine effects. Consequently, the resulting image exhibits unacceptable signal-to-noise (SNR), particularly at the corners of the images. These problems are further aggravated under low light conditions.

Accordingly, there is a strong need in the art for a CMOS image sensor arrangement and method for arranging image sensor elements, which significantly reduces pixel light shadowing.

SUMMARY OF THE INVENTION

The present invention is directed to a CMOS image sensor arrangement and method for arranging image sensor elements which significantly reduce pixel light shadowing. In one exemplary embodiment, the CMOS image sensor comprises a plurality of pixels arranged in an array. The plurality of pixels includes a first pixel proximate an optical center of the array, and a second pixel proximate a peripheral edge of the array. The CMOS image sensor further comprises a first metal interconnect segment associated with the first pixel situated in a first metal layer, and a second metal interconnect segment associated with the second pixel situated in the first metal layer. In accordance with the present invention, the second metal interconnect segment is shifted closer to the optical center of the array than the first metal interconnect segment so that the second metal interconnect segment approximately aligns with a principle ray angle incident the second pixel. The photodiode elements and transistor elements of the pixels of the array remain on a fixed pitch. However, the metal interconnect segments and other pixel elements associated with the pixels of the array are positioned on a variable pitch such that these metal interconnect segments and pixel elements are shifted towards the optical center in proportion to the distance of the metal interconnect segment or associated pixel element from the optical center and in proportion to the distance of the metal interconnect segment or pixel element from the surface of the photodiode.

Thus metal interconnect segments and pixel elements can be positioned at a designated offset position so that the shifts of the metal interconnect segments and pixel elements approximately align to the principle ray angle of the lens incident to the pixel in each location in the array, thereby substantially reducing pixel light shadowing. Proximate the optical center where the principle ray angle is aligned substantially perpendicular to the wafer, the metal interconnect segments are all aligned above the transistor and isolation regions of the pixel leaving the photodiode unobscured to collecting light. In comparison, proximate the corners of the array or proximate the periphery of the array, the metal interconnect segments associated with those pixels

are shifted so as to appear to be "tilted" towards the optical center of the array to thereby align the light collection path with the principle ray angle incident the respective pixels. Such tilts can be typically in the range of 15 to 25 degrees for certain lenses.

This offset positioning (or shift) of the interconnect elements and other pixel elements towards the optical center of the array progressively increases in small intervals at the subsequent pixel placements in proportion to the distance of the pixel from the optical center of the array. These shifts can be applied along a horizontal dimension of the array, a vertical dimension of the array, or along both a horizontal and vertical dimension of the array. With this arrangement the transistor and diode elements of the pixel are always placed in positions corresponding to a fixed pixel pitch interval.

According to another embodiment, the CMOS image sensor further comprises a third metal interconnect associated with the first pixel, and a fourth metal interconnect segment associated with the second pixel, where the third and fourth metal interconnect segment are situated in a second metal layer. In this case, the fourth metal interconnect segment is shifted closer to the optical center than the third metal interconnect segment. Where the first metal layer is situated below the second metal layer, the fourth metal interconnect segment is shifted closer to the optical center than the second metal interconnect segment. These metal interconnect elements may comprise metal lines and vertical via structures to connect the different layers of metal together. In certain embodiments, a first via is situated between the first metal interconnect segment and the third metal interconnect segment, and a second via is situated between the second metal interconnect segment and the fourth metal interconnect segment.

According to another embodiment, the CMOS image sensor further comprises a first micro lens associated with the first pixel, and a second micro lens associated with the second pixel. In this particular embodiment, a second micro lens is shifted closer to the optical center than the first micro lens.

According to another embodiment, the CMOS image sensor further comprises a first color filter associated with the first pixel and a second color filter associated with the second pixel. In this particular embodiment, a second color filter is shifted closer to the optical center than the first color filler.

In another embodiment, the invention is a method for arranging the pixel elements according to the above-described arrangement. Other features and advantages of the present invention will become more readily apparent to those of ordinary skill in the art after reviewing the following detailed description and accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1A** illustrates a top view of a typical CMOS imaging array.

FIG. **1B** illustrates an enlarged view pixel of FIG. **1A**.

FIG. **2A** illustrates a cross sectional-view of a known CMOS imaging array.

FIG. **2B** illustrates the effect of a non-perpendicular principle ray upon a known CMOS imaging array.

FIG. **3A** illustrates a cross sectional-view of a CMOS imaging array in accordance with one embodiment of the present invention.

FIG. **3B** illustrates the effect of a non-perpendicular principle ray upon a CMOS imaging array according to one embodiment of the present invention.

FIG. **4** illustrates a simplified cross-sectional view of camera system in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The present invention is directed to a CMOS image sensor arrangement and method for arranging image sensor elements. The following description contains specific information pertaining to the implementation of the present invention. One skilled in the art will recognize that the present invention may be implemented in a manner different from that specifically discussed in the present application. Moreover, some of the specific details of the invention are not discussed in order to not obscure the invention. The specific details not described in the present application are within the knowledge of a person of ordinary skill in the art.

The drawings in the present application and their accompanying detailed description are directed to merely exemplary embodiments of the invention. To maintain brevity, other embodiments of the invention which use the principles of the present invention are not specifically described in the present application and are not specifically illustrated by the present drawings. It is noted that, for ease of illustration, the various elements and dimensions shown in the drawings are not drawn to scale.

Referring first to FIG. **1A**, a top view of a portion of CMOS imaging array **100** is shown including a plurality of pixels **102**, arranged into rows and columns, each pixel **102** generating photo-charges. The photo-charges generated by pixels **102** are the result of photons striking the surface of the semiconductor material of the photodetector, and generating free charge carriers (electron-hole pairs) in an amount linearly proportional to the incident photon radiation. Pixel **102** in region **104** of imaging array **100** will now be described with reference to FIG. **1B**.

In FIG. **1B**, region **104** and pixel **102** are shown in an enlarged view. Pixel **102** illustrates a three-transistor active pixel design including photodetector **106** (such as a photodiode), reset transistor **108**, source-follower transistor **110**, and select transistor **112**. The active area of transistors **108**, **110** and **112** is depicted as region **114** in FIG. **1B**. In an effort to avoid blocking photodetector **106**, multiple layer metal construction is typically used in CMOS imaging arrays. For example, in FIG. **1B**, metal interconnect segments **116** and **118** are vertically positioned and may, for example, be provided in metal layer two. Metal interconnect segments **120** and **122** are horizontally positioned and may, for example, be provided in metal layer three and metal layer one, respectively. Metal interconnect segments **116** and **118** may be used to provide column selection for both reading and resetting of photodetector **106**. Metal interconnect segment **120** may be used to provide resetting of photodetector **106**, while metal interconnect segment **122** may be used to provide reading of photodetector **106**.

Referring now to FIG. **2A**, a cross sectional-view of known CMOS imaging array **200** is generally shown. Known CMOS imaging array **200** includes pixels **202**, **204** and **206**, wherein pixel **202** is situated in closer proximity to optical center axis **236** than pixel **206**. Optical center axis **236** of imaging array **200** corresponds to a reference line perpendicular to the surface plane of CMOS imaging array **200**, intersecting a center point of CMOS imaging array **200**. By way of illustration, pixel **202** may be situated adjacent or proximate to optical center axis **236**, and pixel **206** may be at or proximate the edge or periphery of known CMOS

imaging array **200**. Each pixel **202** and **206** comprises respective photodetector **208** and **224**, transistor region **210** and **224**, metal one interconnect segments **212** and **226**, metal two interconnect segments **214** and **228**, metal three interconnect segment **216** and **230**, color filter **218** and **232** and micro lens **220** and **234**.

Transistor regions **210** and **224** represent an active pixel design employing a reset transistor, a source follower transistor and a select transistor, as described above in conjunction with FIG. 1B. Respective isolation elements **205** are positioned between transistor regions and photodetectors, e.g., between transistor region **210** and photodetector **108**, and between adjacent pixels, e.g., between pixel **202** and **204**.

In known CMOS imaging array **200**, metal one interconnect segments **212** and **226**, metal two interconnect segments **214** and **228**, and metal three interconnect segments **216** and **230** are routed over respective transistor regions **210** and **224** and isolations regions **205** of pixels **202** and **206**, respectively, to provide electrical connectivity for reading and/or resetting operations involving photodetectors **208** and **222**, respectively, as discussed above.

Color filters **218** and **232** allow light of only specific wavelengths to be transmitted to respective photodetectors **208** and **222**. With the use of color filters, such as filters **218** and **232**, known CMOS imaging array **200** may be used to capture color images. Typically, such color filters are arranged in a repeating Bayer pattern of red, green, and blue filters. Micro lens **220** and **234** are typically formed of a clear polymer and are situated over respective color filters **218** and **232** to redirect light toward respective photodetectors **208** and **222**.

Known CMOS imaging array **200** is configured in a conventional arrangement where each pixel, including pixels **202**, **204** and **206**, are identical in layout and placement of its pixel elements, including corresponding metal interconnect segments, color filters and micro lenses. Stated differently, each pixel **202**, **204** and **206** and its associated pixel elements, i.e., metal interconnect segments, color filter, and micro lens, is identically arranged with a fixed pitch. Thus, dimension **240** defining the placement of the transistor region **210** of pixel **202** is the same as dimension **242** defining the placement of transistor region **224** of pixel **206**. Likewise the dimension **244** and dimension **246** (corresponding to metal one interconnect segments **212** and **226**, respectively) are the same, dimension **248** and **250** (corresponding to metal two interconnect segments **214** and **228**, respectively) are the same, dimension **252** and **254** (corresponding to metal three interconnect segments **216** and **230**, respectively) are the same, dimension **260** and **262** (corresponding to color filters **218** and **232**, respectively) are the same, and dimension **256** and **258** (corresponding to micro lenses **220** and **234**, respectively) are the same. This identical layout scheme is carried out in both the horizontal and vertical dimensions in known CMOS imaging array **200**.

This arrangement of pixel elements in known CMOS imaging array **200** results in significant pixel light shadowing in the resulting image, particularly under low light conditions. As discussed above, pixel light shadowing is caused when the average ray or principal ray striking the pixel deviates significantly from normal (or perpendicular to the imaging array plane). Referring now to FIG. 2B, principal ray **270** and ray bundle **274** are shown having incident angles significantly away from normal or away from perpendicular to imaging array surface **235** of pixel **206**. Ray **270** and ray bundle **274** are redirected by micro lens **234** and passed through color filter **232**. However, because of the initial incident angles of ray **270** and ray bundle **274**, redirected rays **272** and **276** do not strike photodetector **222** but are blocked by pixel elements situated over photodetector **222**, including one or more of metal one interconnect segments **226**, metal two interconnect segments **228** and metal three interconnect segment **230**. A significant amount of illumination will be blocked and prevented from striking photodetector **222** in this manner, resulting in significantly reduced brightness of the resulting image produced by pixel **206**.

Moreover, light incident pixels proximate optical center axis **236**, e.g., pixel **202**, strike surface **235** of those pixels at angles near normal, whereas, pixels near the edge or periphery of known CMOS imaging array **200**, i.e., near the edge of the field of view of the optical system, e.g., pixel **206**, experience an average ray angle which deviates significantly from normal. The resulting image produced by CMOS imaging array **200** thus exhibits significant pixel light shadowing as pixels proximate the edges of the field of view will produce images that have significant and undesirable brightness falls off. This problem is further exacerbated due to the loss of brightness at the edge of field of view common to most lens systems due to 1/Cosine effects. Consequently, the resulting image exhibits unacceptable signal-to-noise (SNR), particularly at the corners of the images. These problems are further aggravated under low light conditions.

Furthermore, as pixels are scaled to smaller pitches to reduced device size, pixel light shadowing becomes even more pronounced as the available area for the photodetector element is reduced. The conventional approach to addressing this problem has been to implement telecentric lenses. Telecentric lenses, however, require more optical elements, thereby increasing the height of the lens, which is undesirable in many applications, such as pocket-sized or portable electronic devices. In addition, the constraints on the optical design of telecentric lenses can result in adverse reduction in Modulation Transfer Function ("MTF"), contrast and other important image quality properties. Finally, telecentric lenses add undesirable increased costs to the camera system, rendering telecentric lenses unpractical in many applications.

Referring now to FIG. 3A, CMOS imaging array **300** which addresses and resolves pixel light shadowing in a simplified and cost-effective manner according to one embodiment of the invention is shown. Pixels **302**, **304** and **306** are shown as part of CMOS imaging array **300** for illustrative purposes, although CMOS imaging array **300** typically include a larger number of pixels. As shown in FIG. 3A, pixel **302** is situated in closer proximity to optical center axis **336** than pixel **306**. Optical center axis **336** of imaging array **300** corresponds to a reference line perpendicular to the surface plane of CMOS imaging array **300**, intersecting a center point of CMOS imaging array **300**. By way of illustration, pixel **302** may be situated adjacent or proximate to optical center axis **336**, and pixel **306** may be at or proximate the edge or periphery of CMOS imaging array **300**.

Each pixel **302** and **306** comprises respective photodetector **308** and **324**, transistor region **310** and **324**, metal one interconnect segments **312** and **326**, metal two interconnect segments **314** and **328**, metal three interconnect segment **316** and **330**, color filter **318** and **332** and micro lens **320** and **334**. As described more fully below, the particular arrangement and placement of metal one interconnect segments **312**

and **326**, metal two interconnect segments **314** and **328**, metal three interconnect segment **316** and **330**, color filters **318** and **332** and micro lenses **320** and **334** of pixels **302** and **306**, respectively, results in significantly reduced pixel light shadowing and superior resulting images.

Transistor regions **310** and **324** represent an active pixel design employing a reset transistor, a source follower transistor and a select transistor, as described above. Respective isolation elements **305** are positioned between transistor regions and photodetectors, e.g., between transistor region **310** and photodetector **308**, and between adjacent pixels, e.g., between pixel **302** and **304**. By way of illustration, isolation elements **305** may comprise shallow trench isolation regions, for example, although other isolation structures may also be used.

Metal one interconnect segments **312** and **326**, metal two interconnect segments **314** and **328**, and metal three interconnect segments **316** and **330** associated with pixels **302** and **306**, respectively, provide electrical connectivity for reading and/or resetting operations involving photodetectors **308** and **322**, respectively, as discussed above. Although not shown in FIG. 3A for ease of illustration, vias are typically positioned to provide vertical interconnections between metal levels corresponding to metal one interconnect segments **312** and **326**, metal two interconnect segments **314** and **328**, and metal three interconnect segments **316** and **330**. Also not shown in FIG. 3A for ease of illustration is a transparent dielectric that supports and encapsulates metal one interconnect segments **312** and **326**, metal two interconnect segments **314** and **328**, and metal three interconnect segments **316** and **330**.

Color filters **318** and **332** allow light of only specific wavelengths to be transmitted to respective photodetectors **318** and **332**. With the use of color filters, such as filters **318** and **332**, CMOS imaging array **300** may be used to capture color images. Typically, such color filters are arranged in a repeating Bayer pattern of red, green, and blue filters. Micro lens **320** and **334** are typically formed of a clear polymer and are situated over respective color filters **318** and **332** to redirect light toward respective photodetectors **308** and **322**.

In accordance with the present invention, the pixel elements, i.e., metal interconnect segments, color filter, micro lens, etc., associated with one or more pixels in CMOS imaging array **300** are physically shifted towards optical center axis **336** in order to approximately align with the principle ray angle incident each pixel. It is noted that the positioning and arrangement of photodetectors **308** and **322** and transistor regions **310** and **324** of pixels **302** and **306**, respectively, are identical and have a fixed pitch. Thus, dimension **340** and **342** are the same.

Referring to FIG. **4**, a simplified cross-sectional view of camera system **400** is shown including image sensor **402** situated on substrate **404**, where, for example, image sensor **402** corresponds to CMOS imaging array **300** of FIG. 3A. Lens holder **406** is positioned over substrate **402** and houses lens assembly **408**. As discussed above, in pocket-sized and portable electronic devices, it is desirable to reduce height **410** of camera system **400**. Thus, maximum principal ray **412** and its incident angle **414** are dependent upon on the various physical dimensions of camera system **400** as well as the position of image sensor **402** on substrate **404**.

Continuing with FIG. 3A, the layout and design of CMOS imaging array **300** can be carried out using a computer program executed on a computer system. For example, the maximum principle ray angle for a particular lens system may be determined by modeling the optical system and pixel performance on the computer system. Once the maximum principle ray angle is determined, the various pixel elements for one or more pixels of CMOS imaging array **300** are shifted toward optical center axis **336** to approximately align with the principle ray angle. According to one embodiment, shifts are applied by using the maximum design grid supported as described more fully below.

By way of illustration, a 22-degree maximum principle ray angle for an f2.8 lens with a +/−10-degree field of view may be defined for a particular camera system employing CMOS imaging array **300**. In accordance with invention, the vertical structure of metal interconnect segments, e.g., metal interconnect segments **312, 314, 316, 326, 328,** and **330**, and the principle ray angle are used to define a required offset or shift in the placement of each of the metal interconnect segments **312, 314, 316, 326, 328,** and **330**, as well as color filters **318** and **332** and micro lenses **320** and **334**. This shift in the metal interconnect segments **312, 314, 316, 326, 328,** and **330**, filters **318** and **332** and micro lenses **320** and **334** is directed toward optical center axis **336**, and, as shown more clearly below, results in significantly reduced blockage of incoming light from being directed at photodetectors **308** and **322**.

The amount of shift for each pixel element is dependent upon the distance of the pixel element from surface **335** of the pixel, the distance of the pixel to optical center axis **336**, and the principle ray angle. By way of example, suppose pixel **306** is situated at the extreme corner of CMOS imaging array **300**, dimension **380** defining the distance between micro lens **334** and photodetector **322** is approximately 5 microns (μm), and the camera system has a principle ray angle of 20-degrees, micro lens **334** is shifted by amount **378** towards the optical center axis **336**. Shift **378** is approximately 0.8 μm depending on the shape of the micro lens and its refractive power. The amount of offset or shift for pixel elements situated below micro lens **334**, e.g., color filter **332**, and metal interconnect segments **326, 328** and **330**, are scaled to a lower value in proportion to the relative distance above photodetector **322**. In the above example, where pixel **306** is at the extreme corner of CMOS imaging array **300**, shift **376** for color filter **332** is approximately 0.64 μm, shift **374** for metal three interconnect segment **330** is approximately 0.48 μm, shift **372** for metal two interconnect segments **328** is approximately 0.32 μm, and shift **370** for metal one interconnect segments **326** is approximately 0.16 μm. Vias (not shown for ease of illustration) which connect metal interconnect segment are also shifted a proportional amount. Thus, any vias connecting metal three interconnect segment **300** and metal two interconnect segment **328** would be shifted by an intermediate value of 0.40 μm, and any vias connecting metal one interconnect segment **326** and metal two interconnect segment **328** would be shifted by an intermediate value of 0.24 μm. It is further noted that, contact structures of transistor regions **324** are not shifted, although the metal one interconnect segment **326** overlap of such contact structures is adjusted to provide adequate overlap between contacts structures and metal one interconnect segment **326** after shifting of metal one interconnect segment **326**. Thus, transistor regions **324**, photodetector **322**, and its respective isolation regions **305** are not shifted.

According to one embodiment, shifts are applied in groups of pixels by an amount equivalent to the supported maximum design grid. For example, in 0.25 micron CMOS, the typical minimum design grid is 0.01 μm. By way of illustration, a VGA imaging array comprises 640 columns and 480 rows of pixels. The number of pixels in each shift group is determined after the maximum shift value is

determined at the edge of the field of view, i.e., for pixels situated at the edge of CMOS imaging array **300**, as described above. If, for example, the maximum shift for a pixel element at the edge or periphery of CMOS imaging array **300** is determined to be 0.8 μm, smaller shifts will be applied in increments of 0.01 μm based upon the radial distance from optical center axis **336**. In the horizontal dimension, for example, there will be 80 groups of shifts, each group including 6 columns (or 6 pixels), each group further away from optical center axis **336** being shifted 0.01 closer to optical center axis **336**. Shifts to the pixel elements are also applied in the vertical dimension of CMOS imaging array **300** in the manner described above.

In general, shifts are applied in greater magnitudes to pixels elements situated further away from optical center axis **336** than pixels structures situated closer to optical center axis **336**. Thus, larger shifts will be applied to metal interconnect segments **326**, **328** and **330** of pixel **306** than metal interconnect segments **312**, **314** and **316** of pixel **302**. Likewise, larger shifts will be applied to color filter **332** and micro lens **334** of pixel **306** than color filter **318** and micro lens **320** of pixel **302**. Referring to metal one segment **326** of pixel **306**, for example, shift **370** indicates that that metal one segment **326** is shifted closer to optical center axis **336** relative to pixel **306** than metal one segment **312** relative to pixel **302**. Thus, dimension **344** of pixel **302** is greater than dimension **346** of pixel **306** by shift amount **370**. Likewise, shift **372** indicates that metal two segment **328** of pixel **306** is shifted closer to optical center axis **336** than metal two segment **314** of pixel **302**, and shift **374** indicates that metal three segment **330** of pixel **306** is shifted closer to optical center axis **336** than metal three segment **316** of pixel **302**. Furthermore, shift **376** indicates that color filter **332** of pixel **306** is shifted closer to optical center axis **336** than color filter **318** of pixel **302**, and shift **378** indicates that micro lens **334** of pixel **306** is shifted closer to optical center axis **336** than micro lens **320** of pixel **302**. It is noted that exceptions to this difference in shift amounts between pixels **302** and **306** arise when pixel elements of pixel **302** and **306** are in the same "shift group," in which case those pixel elements in the same shift group are shifted by the same amount, as noted above.

Also as discussed above, pixel elements situated further above pixel surface **335** are shifted by a greater amount in order to properly align the pixel elements with the principle ray angle. Thus, shift amount **378** is greater than shift amount **376**. Shift amount **378** is in turn greater than shift amount **374**; shift amount **374** is greater than shift amount **372**; and shift amount **372** is greater than shift amount **370**.

Referring to FIG. 3B, principal ray **370** and ray bundle **374** are shown having incident angles significantly away from normal or away from perpendicular to imaging array surface **335** of pixel **306**. Ray **370** and ray bundle **374** are redirected by micro lens **334** and passed through color filter **332**. Due to the particular arrangement of CMOS imaging array **300**, redirected rays **372** and **376** of principal ray **370** and ray bundle **374** strike photodetector **322** but are not blocked by metal interconnect segment **326**, **328** and **330** because each of metal interconnect segments **326**, **328** and **330**, color filter **332**, and micro lens **334** have been shifted toward optical center axis **336** to approximately align with principle ray **370**, as described above. As a result, camera performance is significantly increased, resulting in significant or complete elimination of pixel light shadowing at the edges of CMOS imaging array **300**. According to one embodiment, 25%–50% increases in light collection at the edges of CMOS imaging array **300** is achieved. These benefits are achieved without resort to use of telecentric lenses and its associated disadvantages. Thus, lens size can be reduced, and lens performance is increased. Moreover, since the dimensional tolerance of the manufacturing process is several times greater than a minimum design grid, these small shift or offsets will not interfere with the normal wafer manufacturing process.

From the above description of exemplary embodiments of the invention it is manifest that various techniques can be used for implementing the concepts of the present invention without departing from its scope. Moreover, while the invention has been described with specific reference to certain embodiments, a person of ordinary skill in the art would recognize that changes could be made in form and detail without departing from the spirit and the scope of the invention. For example, it is manifest that the shift amount values and the number of metal interconnect segments described above are merely exemplary and may be modified without departing from the scope and spirit of the invention. The described exemplary embodiments are to be considered in all respects as illustrative and not restrictive. It should also be understood that the invention is not limited to the particular exemplary embodiments described herein, but is capable of many rearrangements, modifications, and substitutions without departing from the scope of the invention.

Thus, a CMOS image sensor arrangement and method for arranging image sensor elements with reduced pixel light shadowing has been described.

What is claimed is:

1. A CMOS image sensor comprising:

a plurality of pixels arranged in an array;

said plurality of pixels including a first pixel proximate an optical center of said array, and a second pixel proximate a peripheral edge of said array;

a first metal interconnect segment associated with said first pixel; and

a second metal interconnect segment associated with said second pixel, wherein said first metal interconnect segment and second metal interconnect segment are situated in a first metal layer, wherein said second metal interconnect segment is shifted closer to said optical center than said first metal interconnect segment so that said second metal interconnect segment approximately aligns with a principal ray angle incident said second pixel.

2. The CMOS image sensor of claim **1**, wherein said second metal interconnect segment is shifted along a horizontal dimension of said array.

3. The CMOS image sensor of claim **1**, wherein said second metal interconnect segment is shifted along a vertical dimension of said array.

4. The CMOS image sensor of claim **1**, wherein said second metal interconnect segment is shifted along both a horizontal and a vertical dimension of said array.

5. The CMOS image sensor of claim **1**, further comprising:

a third metal interconnect segment associated with said first pixel;

a fourth metal interconnect segment associated with said second pixel, wherein said third metal interconnect segment and said fourth metal interconnect segment are situated in second metal layer, wherein said fourth metal interconnect segment is shifted closer to said optical center than said third metal interconnect segment so that said fourth metal interconnect segment approximately aligns with said principal ray striking said second pixel.

6. The CMOS image sensor of claim 5, wherein said first metal layer is situated below said second metal layer, and wherein said fourth metal interconnect segment is shifted closer to said optical center than second metal interconnect segment.

7. The CMOS image sensor of claim 5, further comprising a first via situated between said first metal interconnect segment and said third metal interconnect segment.

8. The CMOS image sensor of claim 7, further comprising a second via situated between said second metal interconnect segment and said fourth metal interconnect segment.

9. The CMOS image sensor of claim 1, further comprising:

a first micro lens situated associated with said first pixel; and

a second micro lens associated with said second pixel, wherein said second micro lens is shifted closer to said optical center than said first micro lens.

10. The CMOS image sensor of claim 1, further comprising:

a first color filter associated with said first pixel; and

a second color filter associated with said second pixel, wherein said second color filter is shifted closer to said optical center than said first color filter.

11. A CMOS imaging array comprising:

a plurality of pixels arranged in rows and columns, each said pixel including a photodetector;

said plurality of pixels including a first pixel proximate an optical center of said CMOS imaging array, and a second pixel proximate a peripheral edge of said array;

a first metal interconnect segment associated with said first pixel; and

a second metal interconnect segment associated with said second pixel, wherein said first metal interconnect segment and second metal interconnect segment are situated in a first metal layer, wherein said second metal interconnect segment is shifted closer to said optical center than said first metal interconnect segment so that said second metal interconnect segment approximately aligns with a principal ray angle incident a photodetector of second pixel.

12. The CMOS imaging array of claim 11, wherein each of said first and second transistor regions comprises a respective reset transistor, a respective source-follower transistor, and a respective select transistor.

13. The CMOS imaging array of claim 11, wherein said photodetector is a photodiode.

14. The CMOS imaging array of claim 11, wherein said second metal interconnect segment is shifted along at least one of a horizontal or a vertical dimension of said array.

15. A CMOS imaging array of a lens system having a principle ray angle, said CMOS imaging array comprising:

a plurality of pixels including a first pixel, said first pixel having a photodetector;

at least a first micro lens element associated with said first pixel, said first micro lens element having a first offset position;

wherein said first pixel is situated at a periphery of said imaging array, and wherein said first micro lens element is fabricated at said first offset position so that said micro lens element approximately aligns with said principle ray angle incident said first pixel.

16. The CMOS imaging array of claim 15 further comprising:

a first color filter associated with said first pixel, said first color filter having a second offset position;

wherein said second offset position is derived by proportionally scaling said first offset position according to a distance of said first color filter above said photodetector relative to a distance of said first micro lens element above said photodetector;

wherein said first color filter is fabricated over said photodetector at said second offset position, and said first micro lens is fabricated over said first color filter.

17. The CMOS imaging array of claim 15 further comprising:

a first metal interconnect segment associated with said first pixel, said first metal interconnect segment having a second offset position;

wherein said second offset position is derived by proportionally scaling said first offset position according to a distance of said first metal interconnect segment above said photodetector relative to a distance of said first micro lens element above said photodetector;

wherein said first metal interconnect segment is fabricated over said photodetector at said second offset position.

18. The CMOS imaging array of claim 17, further comprising:

a second metal interconnect segment associated with said first pixel, said second metal interconnect segment having a third offset position;

wherein said third offset position is derived by proportionally scaling said first offset position according to a distance of said second metal interconnect segment above said photodetector relative to a distance of said first micro lens element above said photodetector.

19. The CMOS imaging array of claim 18, wherein said second metal interconnect segments is fabricated above said first metal interconnect segment, said third offset position in closer proximity to an optical center axis of said imaging array than said second offset position.

20. The CMOS imaging array of claim 19 further comprising:

a via fabricated between said first metal interconnect segment and said second metal interconnect segment, said via having a fourth offset position having an intermediate position between said second offset position and said third offset position.

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